MODULE 1

SEMICONDUCTOR DIODES AND APPLICATIONS

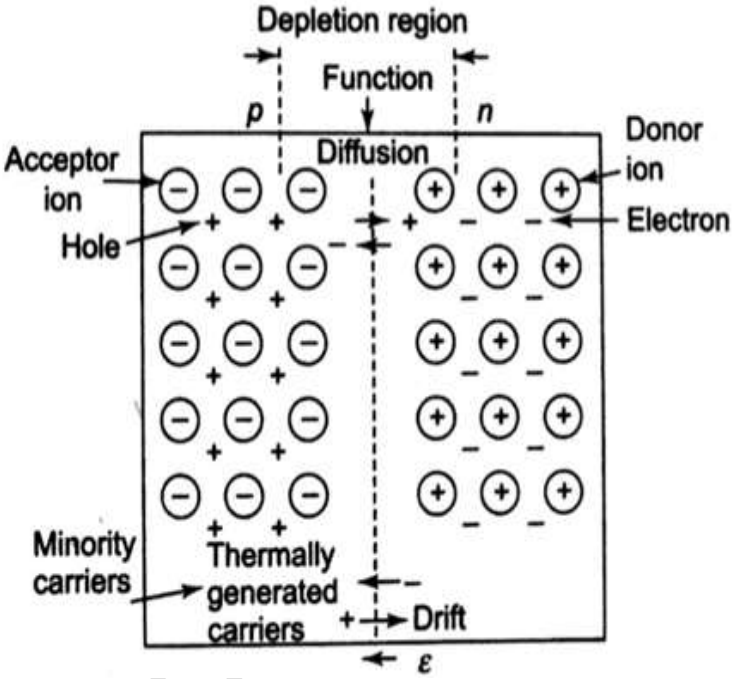
Diode: A diode is a semiconductor device which eases conduction in one direction and stops conduction in other direction. It has two terminals namely Anode and Cathode.

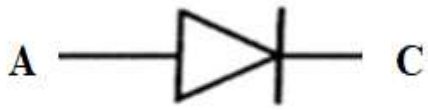
It has wide range of applications like;

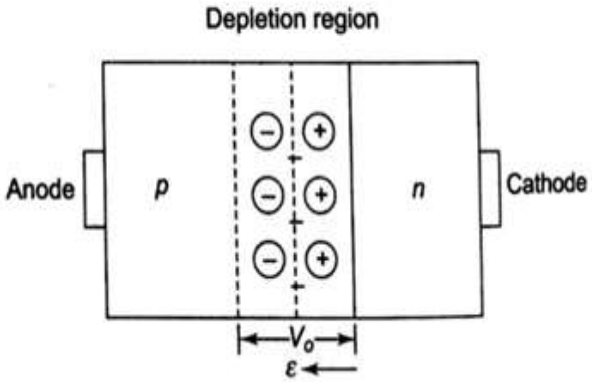
i. Rectification
ii. Voltage Regulation
iii. Wave Shaping etc.

PN- Junction Diode:

Construction:







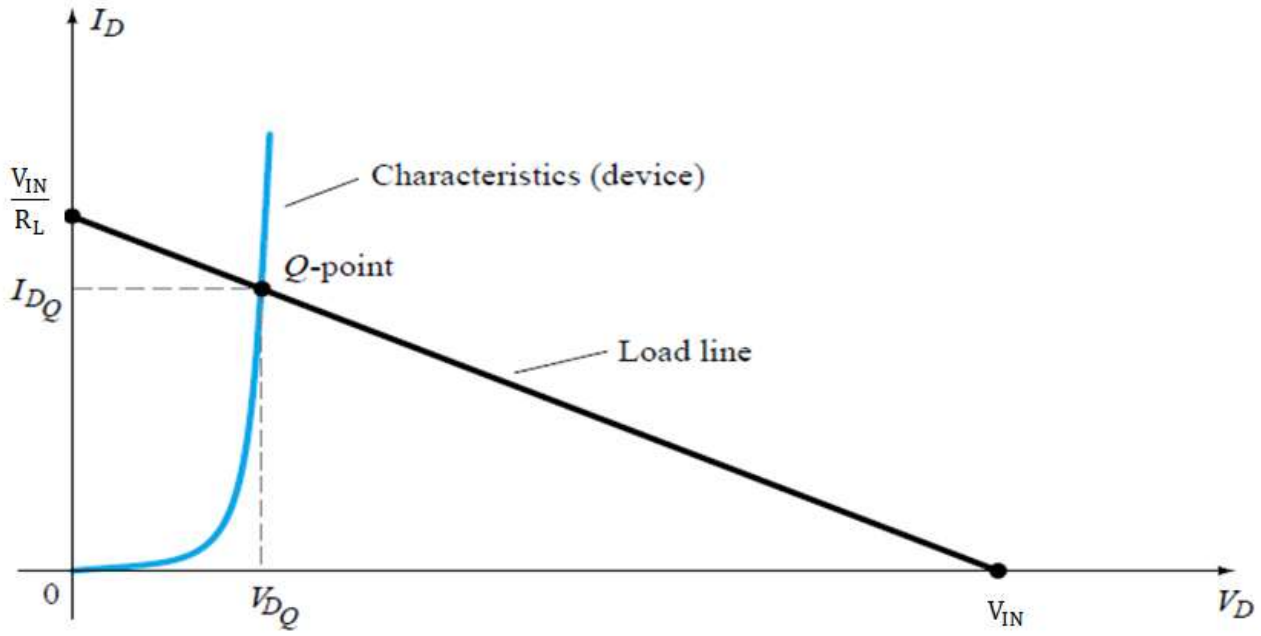
- When a thin layer of P-type semiconductor and N-type semiconductor are placed together, a junction in formed called as PN junction.
- The P-side is called Anode [A] and the N-side is called Cathode [C].
- Majority holes from P-side diffuses (moves) to N-side and Majority electrons from N-side diffuses (moves) to P-side.
- Recombination of holes and electrons forms a narrow region on both side of the junction which forms fixed positive ions at N-side and negative ions at P-side.
- This region is called ***Depletion Region*** where no free electrons and holes are present.
- At the junction an electric field is created which opposes the flow of charges.
- In steady state, there is no net current flow across junction.

Operation: [DC Load Line analysis]:

- Consider the simple diode circuit as shown above which consist of dc voltage source, diode and a load resistor.
- A DC input voltage $\mathbf{V_{in}}$ is applied to the diode. The output is the voltage across the load resistor R_L.
- Diode is said to be forward biased and current $\mathbf{I_D}$ flows in the circuit.
- Applying KVL to the circuit.

$$+V_{IN} - V_D - V_{RL} = 0$$
$$V_{IN} = V_D + V_{RL}$$
$$\text{OR} \quad V_D = V_{IN} - V_{RL}$$
$$V_D = V_{IN} - (I_D * R_L)$$

- The above equation is called as dc load line equation.
- Assuming $\mathbf{R_L = 0}$, We get $V_D = V_{IN}$
- Assuming $V_D = 0$, We get $I_D = \frac{V_{IN}}{R_L}$
- Now we have two points on the characteristic curve. When those two points are joined, we get a straight line which intersects the characteristic curve.
- The point of intersection of Load line and the characteristic curve is called as Q-Point, i.e. quiescent point or Operating Point.



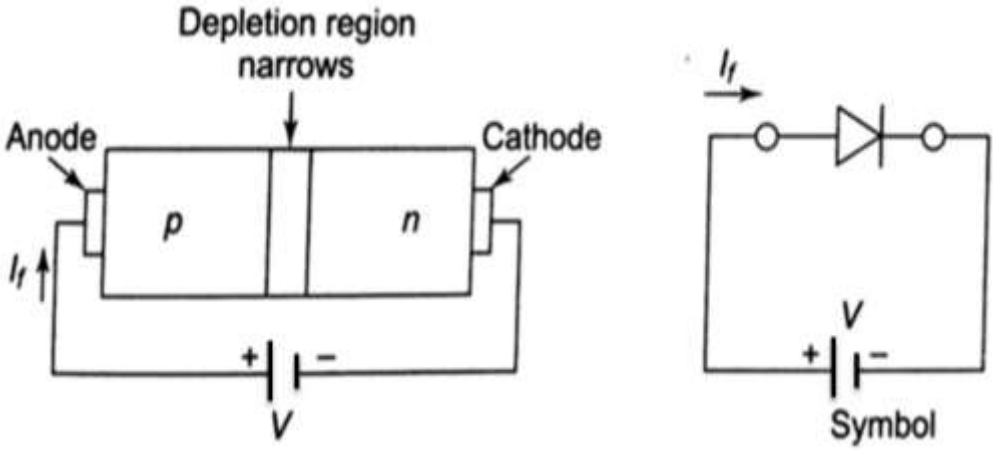
Drawing the load line and finding the point of operation.

Biasing:

Applying an external voltage to a device is called Biasing. There are two types of biasing;

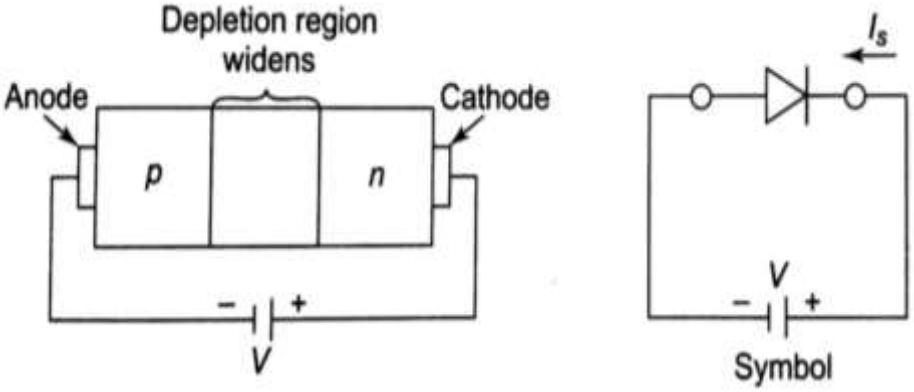
1. Forward Biasing
2. Negative Biasing

Forward Biasing of Diode:

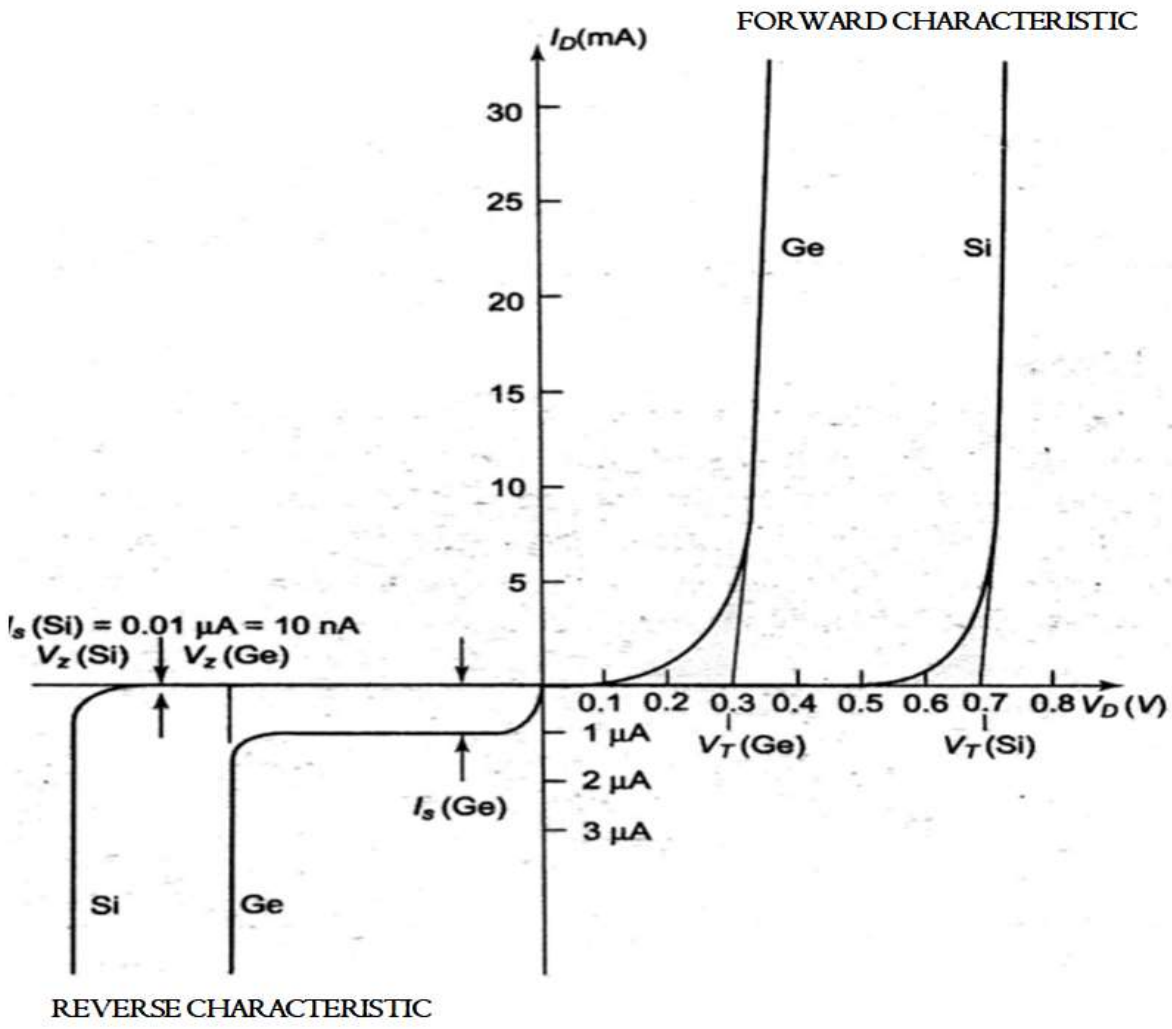


1. When the positive terminal of the battery is connected to the Anode (P-side) and negative terminal is connected to the Cathode (N-side), diode is said to be forward biased.
2. The holes from P-type and electrons from N-type are moved towards the junction, reducing the depletion region.
3. Hence, holes moves towards N-side and electrons moves towards P-side easily which produces the Current in the diode $\mathbf{I_d}$ (Diode Current)

Reverse Biasing of Diode:



1. When the negative terminal of the battery is connected to the Anode (P-side) and positive terminal is connected to the Cathode (N-side), diode is said to be forward biased.
2. As a result of reverse biasing, the majority of holes and electrons are pulled away from the junction, which increases the width of the depletion region.
3. Therefore majority charge carrier current cannot flow, but minority carrier drift current flows which stays at saturation level which is very low.
4. Reverse Saturation Current $\mathbf{I_s}$ will be in negligible order.



Diode Relationship:

$$I_D = I_S\,(e^{kV_D/T_k} - 1)$$

Where; I_s = Reverse Saturation Current
k = 11,600 / η ; η = 1 for Ge and η = 2 for Si for Low Current. η = 1 for both Ge and Si for higher level of current.
$T_k = T_c + 273^0$; T_c = Operating Temperature 25^0

- The Plots for Ge and Si diodes are drawn to scale in the figure below.
- The sharply rising part of the curve extended downwards meets the V_D axis which is indicated by $\mathbf{V_T}$ and referred as ***Threshold Voltage.***
- It is assumed that I_D = 0 upto V_T and then increases linearly. V_T=0.7 V for Si diode and V_T=0.3 for Ge diode.

Zener Region:

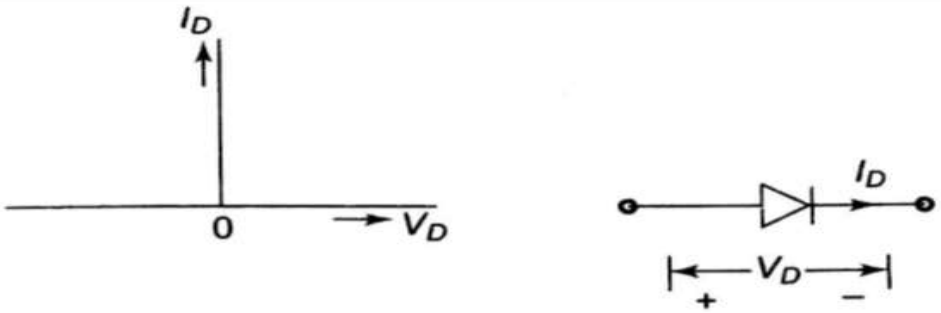
1. As the revers-bias voltage is raised, the diode breaks down at the Voltage $\mathbf{V_z}$ by Avalanche Phenomenon.
2. The maximum negative voltage that a diode can withstand is called Peak Inverse Voltage. [PIV].

Zener Breakdown:

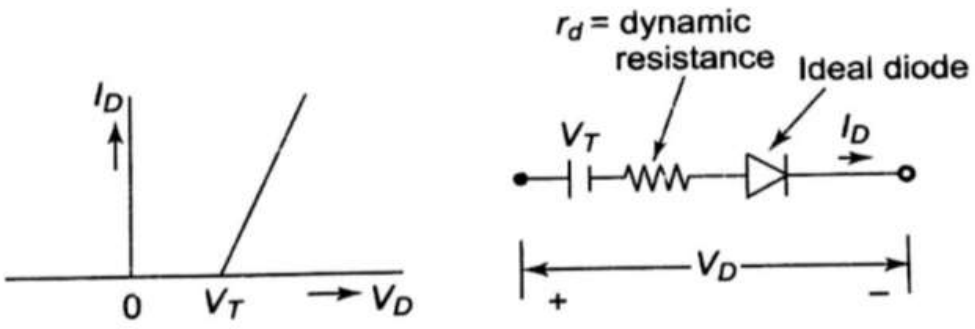
1. By heavily doping the N and P regions, the break down voltage Vz can be brought as low as -10 V, -5 V.
2. This break down is different from avalanche. This type of diode is called Zener Diode.
3. This diode does not allow the potential there to exceed the diode rated voltage.

Equivalent Circuit:

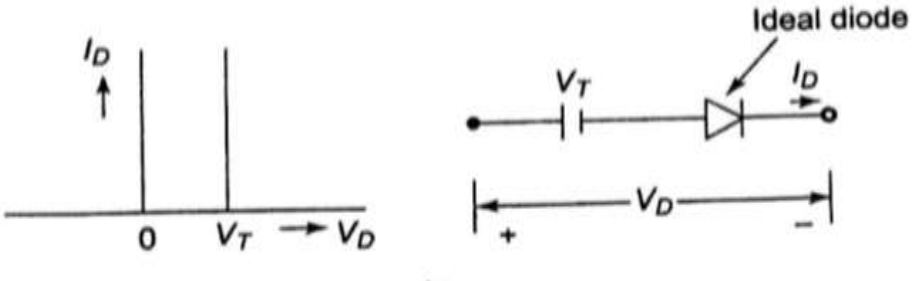
1. ***Ideal Diode:*** Diode which conducts when $\mathbf{V_D} > 0$ are called ideal diode.



2. ***Piecewise Linear Model:*** In this model, we consider the Diode Resistance ($\mathbf{r_d}$ _ Dynamic Resistance) with applied voltage above threshold voltage $\mathbf{V_T}$

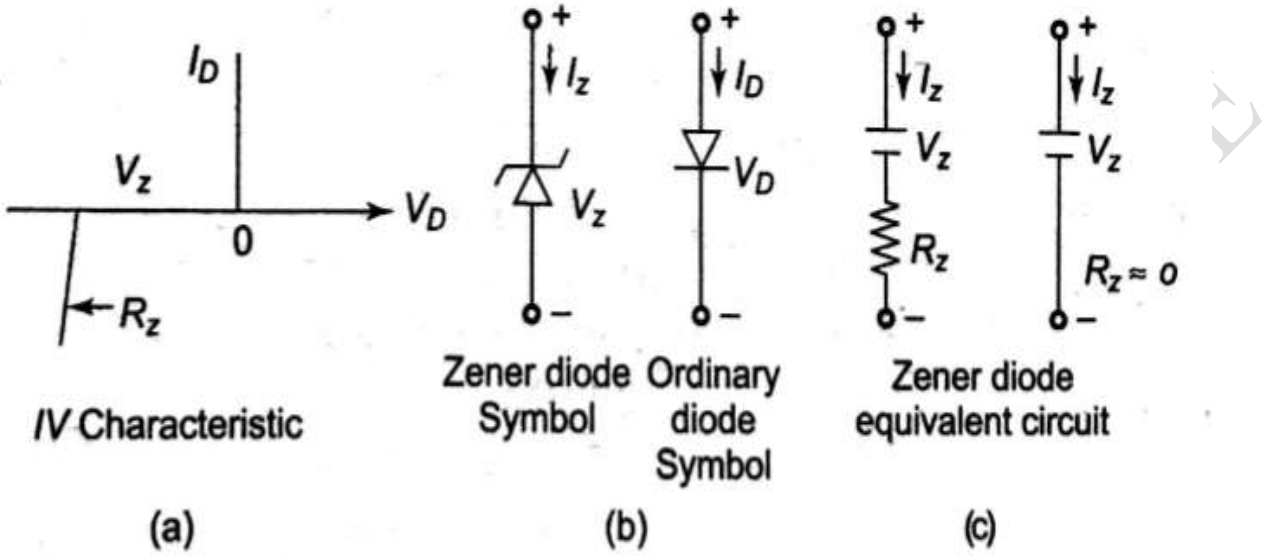


3. ***Approximation Model:*** Assuming rd = 0, the model characteristic and circuit are drawn as shown below.



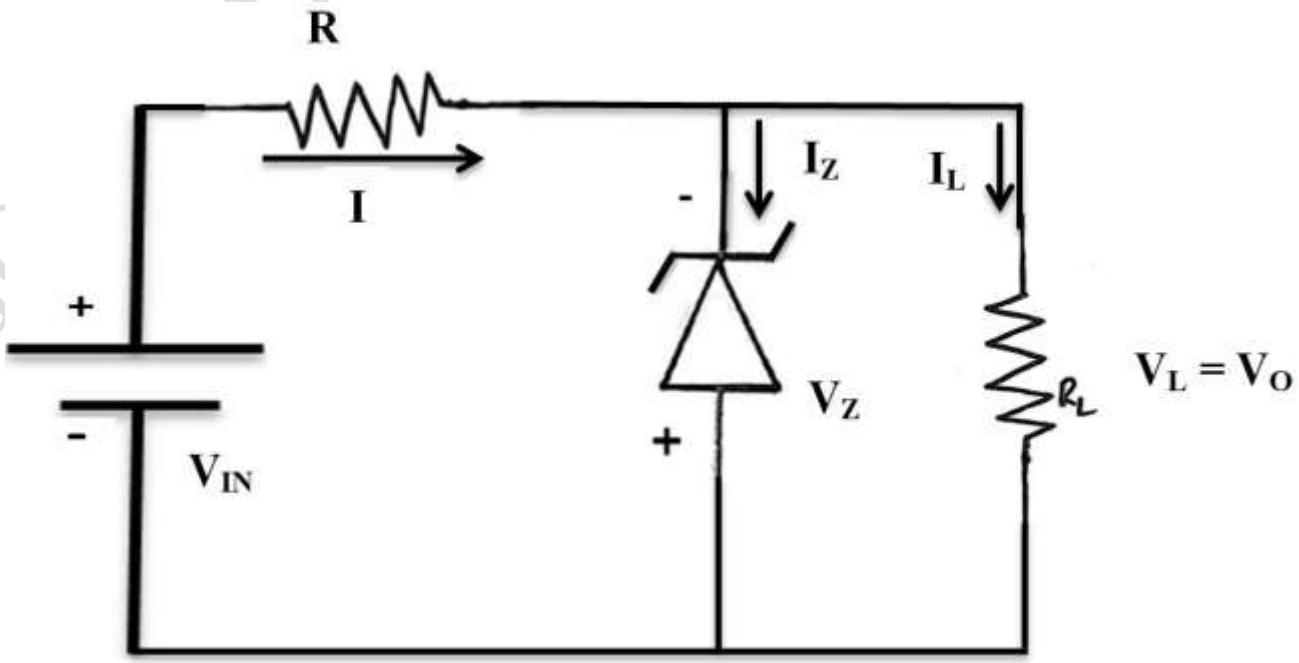
Zener Diode:

- A Zener diode has zero breakdown in reverse bias as shown in VI characteristics of figure **a**.
- The symbol of the Zener diode is drawn in figure **b.** Its equivalent circuit is drawn in figure **c.**
- It is connected in circuit such that it is reverse biased. It conducts only if reverse bias exceeds $\mathbf{V_z}$.



Zener Diode as a Voltage Regulator:

- Voltage regulators are the devices used to maintain constant voltage across load despite of fluctuations in the input voltage and load current.
- The Zener diode in its reverse region is widely used as voltage regulator as it continues to operate till the magnitude of current becomes less than $I_{Z(min)}$.
- The typical Zener voltage regulator is shown in figure below.
- The Zener diode of breakdown voltage V_Z is connected to the input supply in reverse direction.
- For all the values of current within the breakdown region, the voltage across the diode will remain fixed at V_Z, giving a constant supply across its load.
- The resistance R_S controls the current flowing in the circuit.



1. ***Line Regulation:*** *[Input voltage is varied and Load resistance is kept constant]*

- In this case, **load resistance is kept constant** and **input voltage (V_{in}) is varied.**
- The regulated output voltage is achieved for input voltage above certain minimum level.

It can be seen that the output is $\mathbf{V_O = V_Z}$ is constant.

$\mathbf{I_L}$ is given by; $$\mathbf{I_L = \frac{V_O}{R_L} = \frac{V_Z}{R_L} = constant}$$

Total current $\mathbf{I}$ is given by: $$\mathbf{I = I_Z + I_L}$$

Now if $\mathbf{V_{in}}$ **increases**, then the total current **I increase**. But $\mathbf{I_L}$ is constant as $\mathbf{V_Z}$ is constant. Hence the current $\mathbf{I_Z}$ **increases** to keep $\mathbf{I_L}$ constant. (I_L is constant, I increases, I_Z becomes Maximum (I_{Zmax})).

For $\mathbf{V_{in}}$**= Maximum**; $\mathbf{I = I_{Zmax} + I_L}$ $\mathbf{I_{Zmax} = I - I_L}$

Now if $\mathbf{V_{in}}$ **decreases**, then the total current **I decrease**. Since $\mathbf{V_Z}$ is constant, hence the current $\mathbf{I_Z}$ **decreases** to keep $\mathbf{I_L}$ **constant**. (I_L is constant, I decreases, I_Z becomes Minimum (I_{Zmin}))

For $\mathbf{V_{in}}$**= Minimum**; $\mathbf{I = I_{Zmin} + I_L}$ $\mathbf{I_{Zmin} = I - I_L}$

As long the $\mathbf{I_Z}$ value is between $\mathbf{I_{Zmin}}$ and $\mathbf{I_{Zmax}}$, output voltage $\mathbf{V_O}$ will be constant.

2. ***Load Regulation*****:** *[Load resistance is varied and Input voltage is kept constant]*

- In this case **the input voltage is fixed** while the **load resistance is varied**.
- The constant output voltage is obtained as long as the load resistance is maintained above a minimum value.

Since $\mathbf{V_O = V_Z}$ is constant, then for constant $\mathbf{R}$, $\mathbf{I}$ is given by $\mathbf{I = \frac{V_{in} - V_z}{R} = I_Z + I_L}$

Now if $\mathbf{R_L}$ **decreases**, then $\mathbf{I_L}$ **increases**, to keep **I constant,** $\mathbf{I_Z}$ **decreases**. (I_L increases, I_Z becomes Minimum (I_{Zmin})).

For $\mathbf{R_L}$**= Minimum;**

$\mathbf{I_L}$ **is Maximum** $\mathbf{I = I_Z + I_{Lmax}}$ $\mathbf{I_{Zmin} = I - I_{Lmax}}$

Now if $\mathbf{R_L}$ **increases**, then $\mathbf{I_L}$ **decreases**, to keep **I constant,** $\mathbf{I_Z}$ **increases**. (I_L decreases, I_Z becomes Maximum (I_{Zmax})).

For $\mathbf{R_L}$**= Maximum;**

$\mathbf{I_L}$ **is Minimum** $\mathbf{I = I_Z + I_{Lmin}}$ $\mathbf{I_{Zmax} = I - I_{Lmin}}$

As long the I_Z value is between I_{Zmin} and I_{Zmax}, output voltage V_O will be constant.

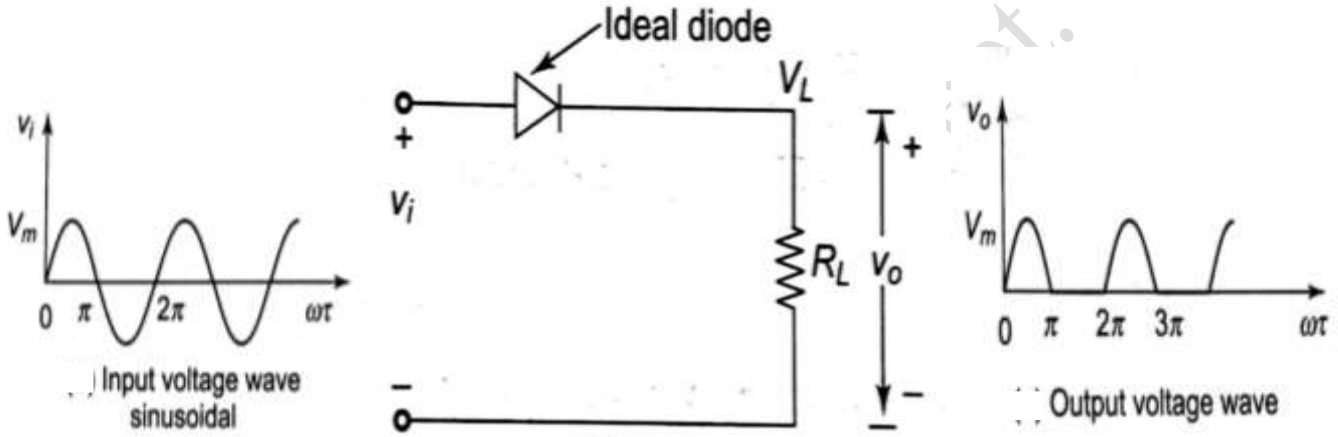
Rectification:

The process of converting AC to DC is called Rectification. An diode is an ideal and simple device to convert AC to DC.

Here we measure the different parameters of DC voltage:

1. DC Voltage
2. Ripple Factor
3. Power Conversion Efficiency
4. PIV

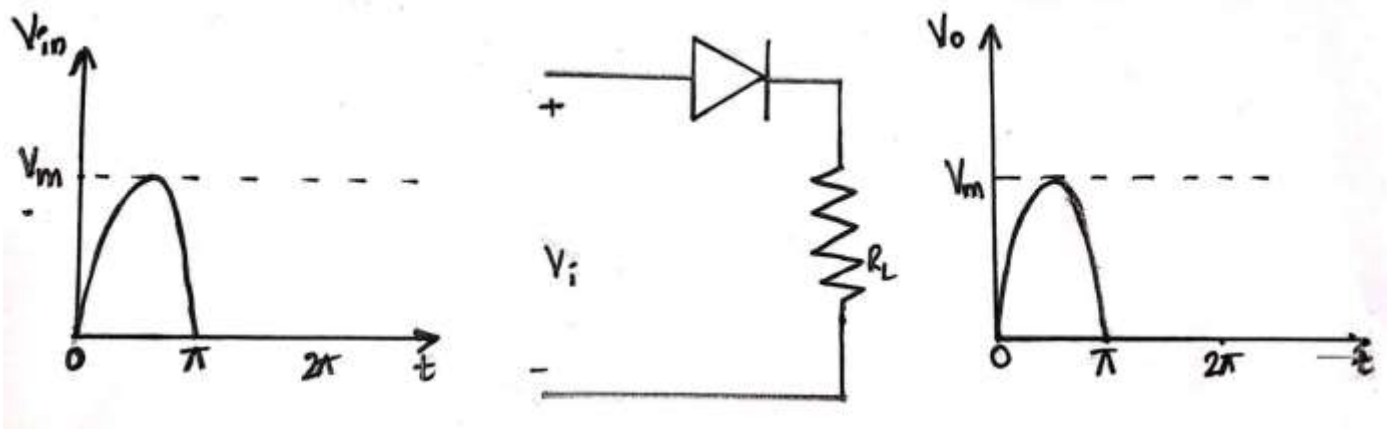
Half-Wave Rectification:



1. A Half-wave rectifier circuit consists of a diode and a resistor.
2. The diode conducts during the positive half cycles of the input and cuts off during the negative half cycles.

3. **For the period:** $\mathbf{0 - \pi}$

a. We get positive half cycle of the sinusoidal input.
b. The diode gets forward biased and it conducts producing the output for the same period.

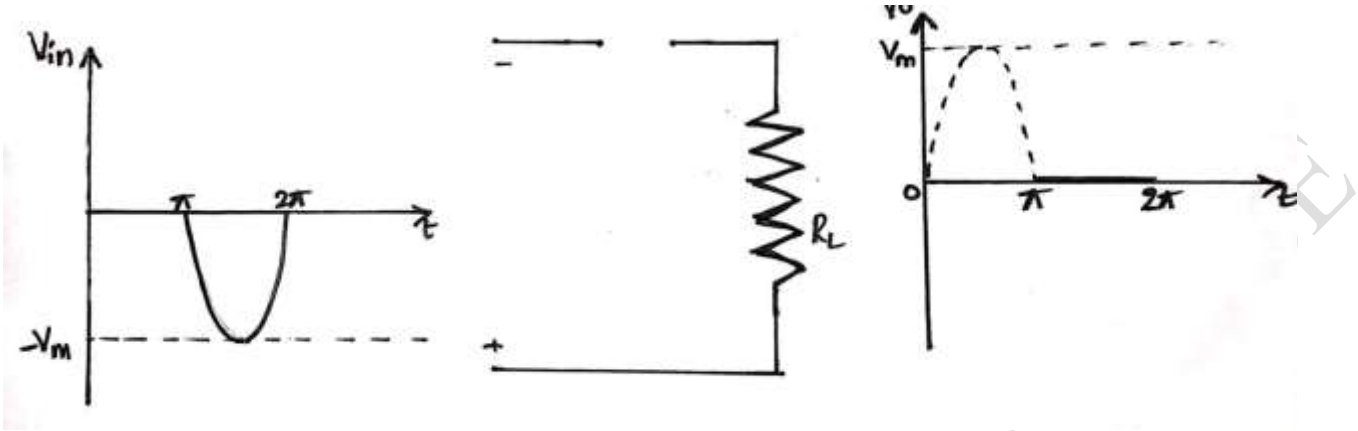


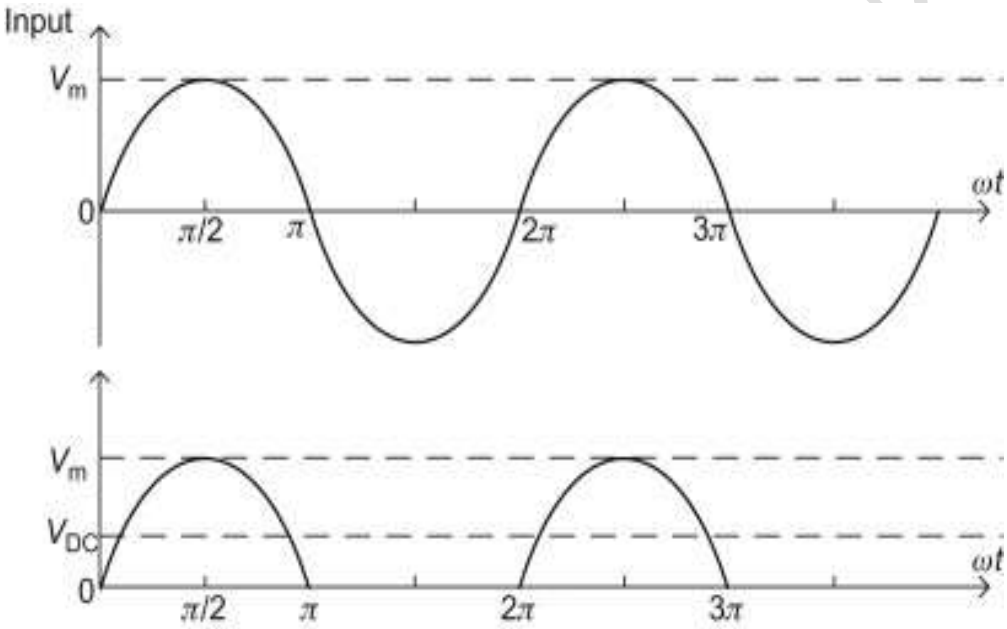
4. **For the period:** $\pi - 2\pi$

a. We get the negative half cycle of the sinusoidal input.

b. The diode gets reverse biased and it does not conduct and the output is zero for the same period.

5. The input output waveform is as shown below.





Output Voltage:

$$V_{dc} = \frac{1}{2\pi}[\, V_m \int_0^{\pi} sin\omega t \, d\omega + 0 \,]$$

$$\mathbf{V_{dc}} = \frac{V_m}{\pi} = 0.318 * V_m$$

Current: $\mathbf{I_{dc}} = \frac{V_m}{\pi} * \frac{1}{R_L} = \frac{I_m}{\pi} = 0.318 * I_m$

$$\mathbf{I_{dc}} = 0.318 * I_m$$

PIV for half wave rectifier is: **PIV = $\mathbf{V_m}$**

Ripple Factor of Half Wave Rectifier:

Ripple is the variation of the output voltage about DC, which is high in Half-rectified wave.

It has the frequency twice the frequency of the input voltage wave.

$$\textbf{Ripple Factor} \quad \gamma = \frac{rms\ value\ of\ the\ AC\ component\ of\ Load\ Voltage}{DC\ component\ of\ load\ voltage}$$

$$\gamma = \sqrt{\frac{V_{L\,rms}^2}{V_{L\,dc}^2} - 1}$$

$V_{L\,rms}$ = rms of half sine wave (0- π) over (0-2 π)

$$V_{L\,rms} = \sqrt{\frac{V_m}{\sqrt{2}}^2 * \frac{1}{2}}$$

$$V_{L\,rms} = \frac{V_m}{2}$$

$$\gamma = \sqrt{\frac{(V_m/2)}{(V_m/\pi)^2}^2 - 1}$$

$$= \left[\left(\frac{\pi}{2}\right)^2 - 1\right]^{1/2}$$

$$= 1.21$$

We find that ripple factor of an half wave rectifier is quite higher, which is unacceptable. It is adjusted by the transformer output.

Power Conversion Efficiency of Half Wave Rectifier:

It is defined as the ratio of DC power output and the AC power input.

$$\eta = \frac{DC\ Power\ Output}{AC\ Power\ Input}$$

DC Output = $I_{dc}^2 * R_L$

AC Input = $I_{rms}^2 * R_L$

$$I_{rms} = \sqrt{\frac{I_m}{\sqrt{2}}^2 * \frac{1}{2}}$$

$$I_{rms} = \frac{I_m}{2}$$

$$\eta = \left[\frac{I_{dc}}{I_{rms}}\right]^2$$

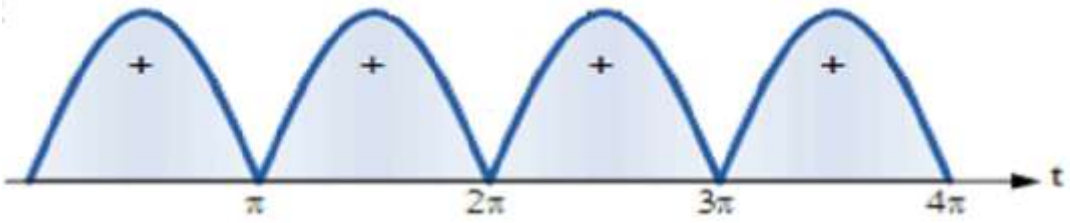
$$\eta = \left(\frac{I_m/\pi}{I_m/2}\right)^2$$

$$= (2/\pi)^2$$

$$= 0.405 \quad \text{or} \quad 40.5\%$$

Full Wave Rectification:

1. In order to reduce the ripple factor and raise the output dc voltage level, we switch to full-wave rectification.
2. Here we get the output for the complete one cycle of the input.
3. At the output, phase of the second half of the wave is reversed.
4. The full wave rectified output is as shown below:



$$\mathbf{V_{DC} = \frac{2V_m}{\pi} = 0.637\ V_m}$$

$$\mathbf{I_{DC} = \frac{2I_m}{\pi}} \qquad \mathbf{I_m = (V_m/R_L)}$$

Ripple Factor of Full Wave Rectifier:

$$V_{L\,rms} = \frac{V_m}{\sqrt{2}}$$

$$\gamma = \sqrt{\frac{(V_m/\sqrt{2})^2}{(2\,V_m/\pi)^2} - 1}$$

$$= \left[\frac{\pi^2}{8} - 1\right]^{1/2}$$

$$\gamma = 0.482$$

Power Conversion Efficiency of Full Wave Rectifier:

DC Output = $I_{dc}^2 * R_L$

AC Input = $I_{rms}^2 * R_L$

$$I_{rms} = \frac{I_m}{\sqrt{2}}$$

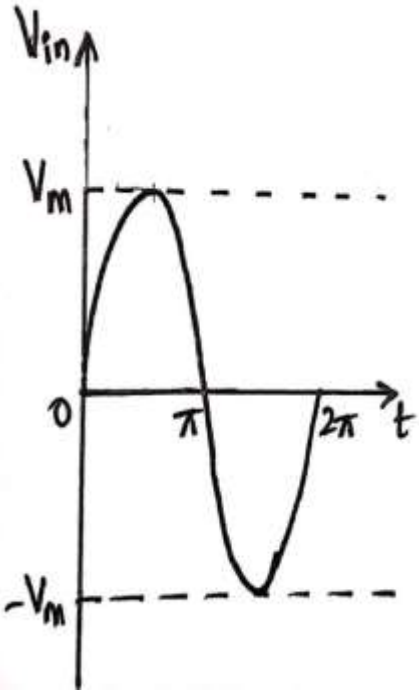
$$\eta = [\frac{I_{dc}}{I_{rms}}]^2$$

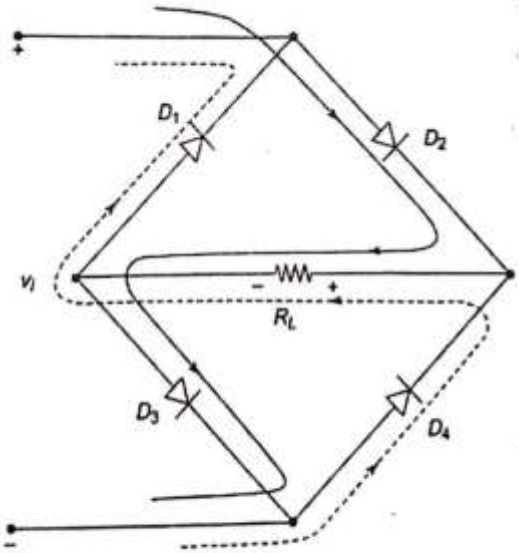
$$\eta = (\frac{2I_m/\pi}{I_m/\sqrt{2}})^2$$

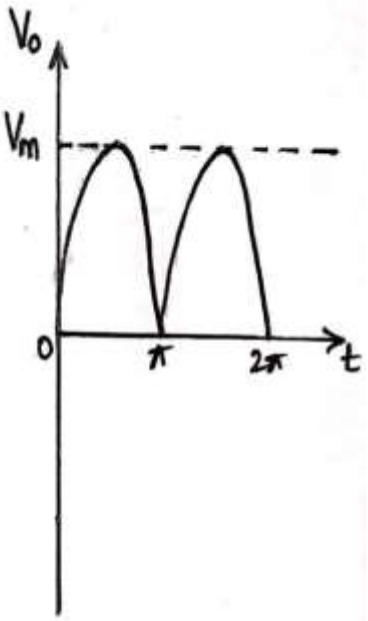
$$= (2\sqrt{2}/\pi)^2$$

$$= 0.81 \text{ or } 81\%$$

Bridge Rectifier:

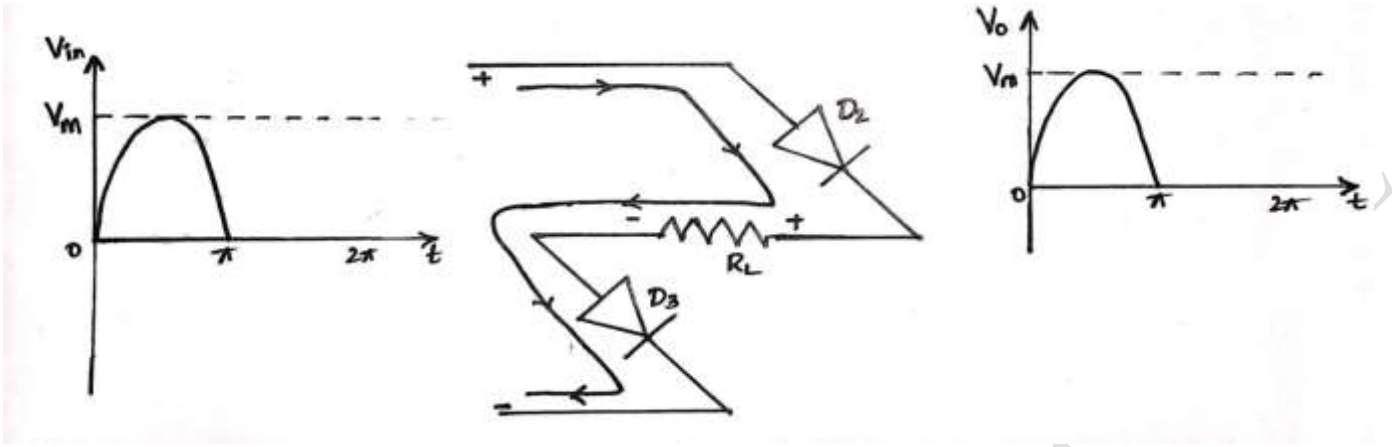




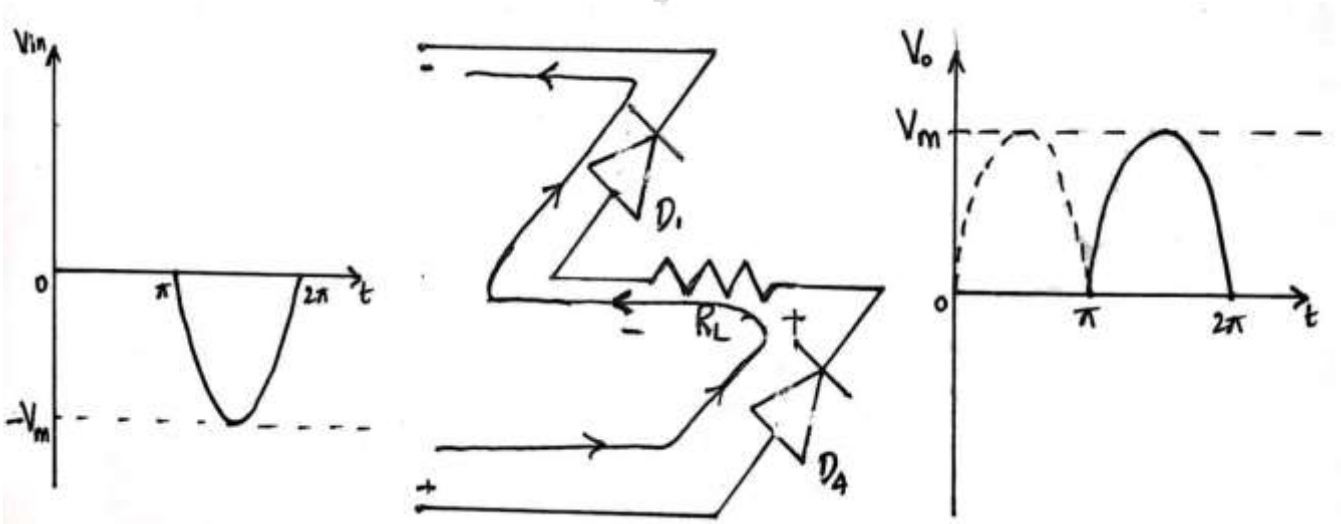


1. The circuit consists of 4 diodes which forms the bridge structure. It is the most common full-wave rectifier circuit used.

2. **During the period of: 0- π**
   a. We get positive half cycle of the sinusoidal input.
   b. The diodes $\mathbf{D_2}$ and $\mathbf{D_3}$ gets forward biased and it conducts through $\mathbf{R_L}$ producing the output for the same period. Diodes $\mathbf{D_1}$ and $\mathbf{D_4}$ gets reversed biased and it will be in the OFF state.

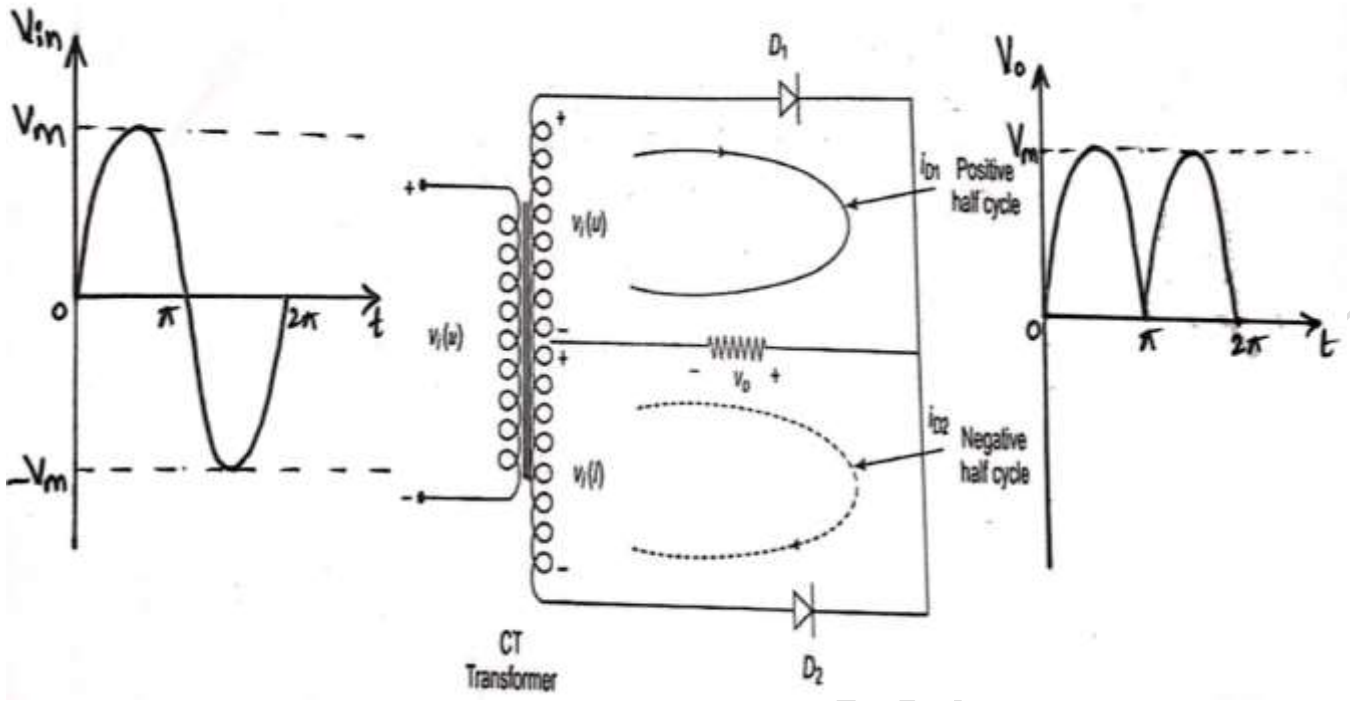


3. **During the period of: π - 2π**
   a. We get negative half cycle of the sinusoidal input.
   b. The diodes $\mathbf{D_1}$ and $\mathbf{D_4}$ gets forward biased and it conducts through $\mathbf{R_L}$ producing the output for the same period. The diodes $\mathbf{D_2}$ and $\mathbf{D_3}$ get reversed biased and it will be in the OFF state.
4. Since the direction of flow of current through load resistance $\mathbf{R_L}$ remains same for both the half cycles, we get the positive output at $\mathbf{R_L}$



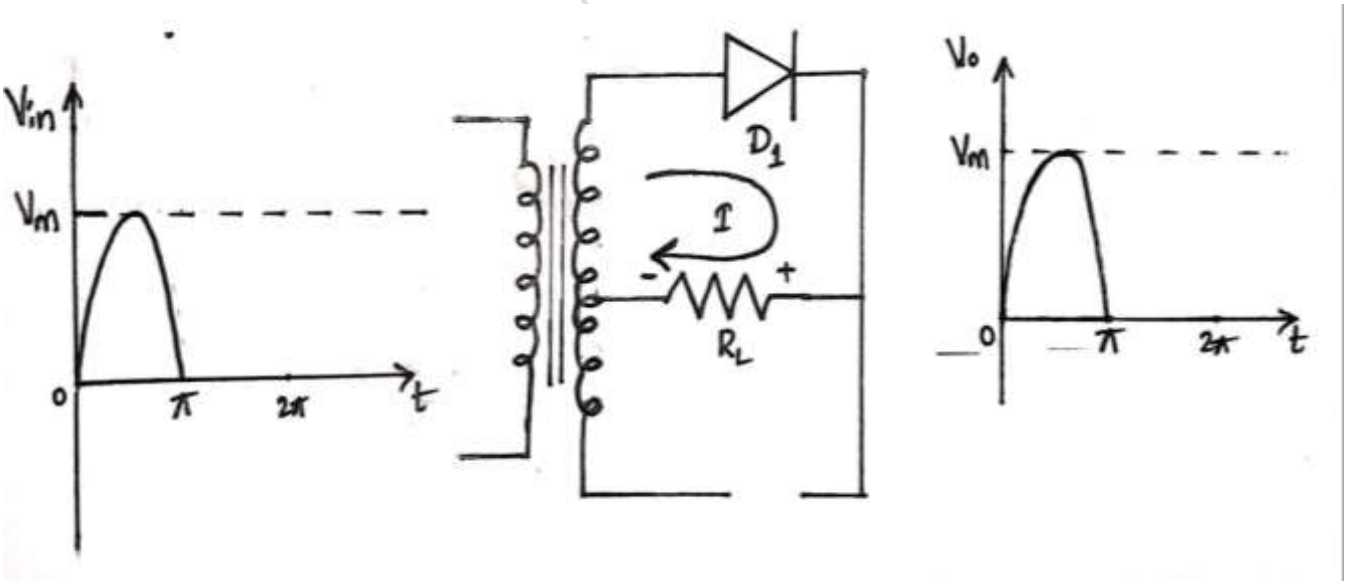
PIV for Bridge Rectifier is: **PIV > $\mathbf{V_m}$**

Rectifier using Centre-Tapped (CT) Transformer:

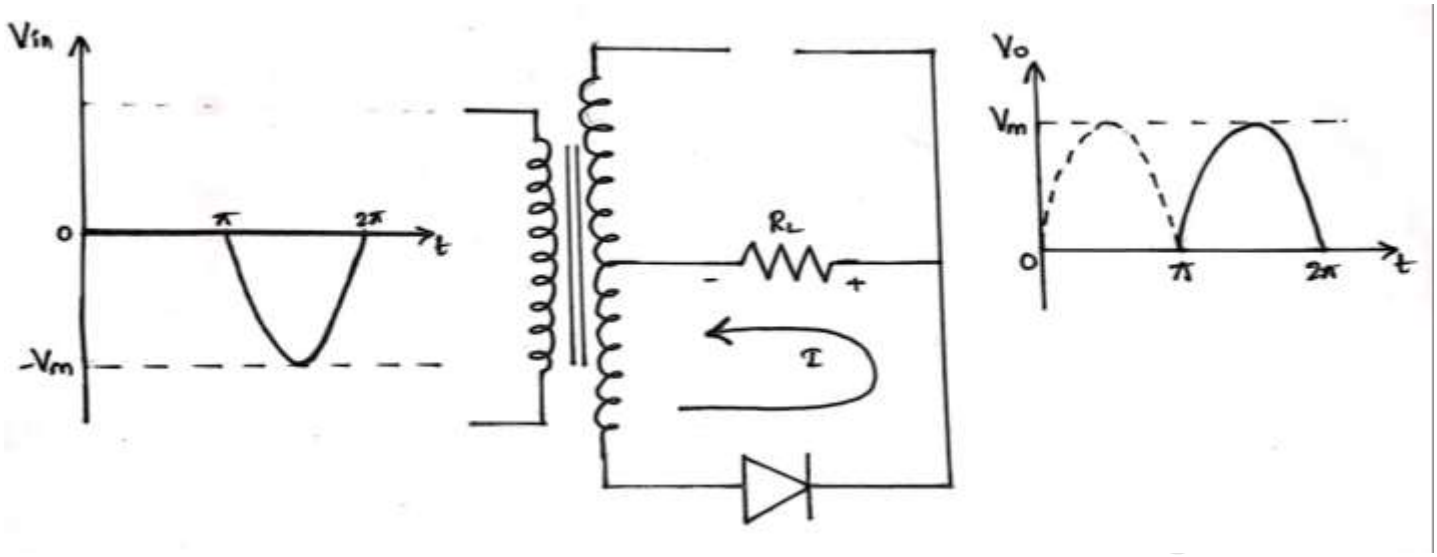


1. The circuit consists of two diodes with a Centre Tapped transformer. The network is as shown in the figure.

2. **During the period of: 0- π**
   a. We get positive half cycle of the sinusoidal input.
   b. The diodes $\mathbf{D_1}$ gets forward biased and it conducts through $\mathbf{R_L}$ producing the output for the same period. Diodes $\mathbf{D_2}$ gets reversed biased and it will be in the OFF state.



3. **During the period of: π - 2π**
   a. We get negative half cycle of the sinusoidal input.
   b. The diodes $\mathbf{D_2}$ gets forward biased and it conducts through $\mathbf{R_L}$ producing the output for the same period. The diodes $\mathbf{D_1}$ get reversed biased and it will be in the OFF state.

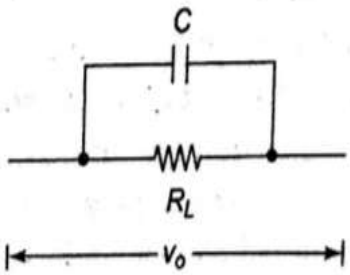


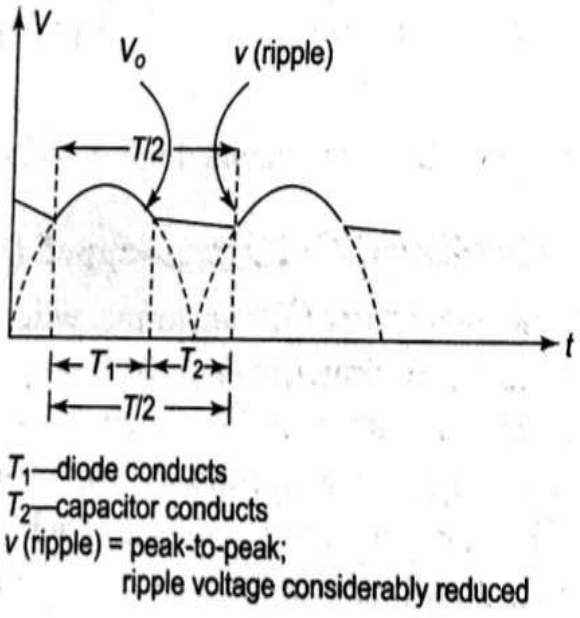
4. Since the direction of flow of current through load resistance $\mathbf{R_L}$ remains same for both the half cycles, we get the positive output at $\mathbf{R_L}$.

PIV voltage of Centre Tapped Transformer is: **PIV > $2V_m$**

Filtering:

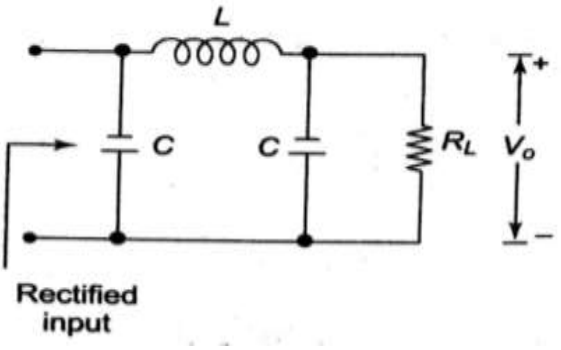
- Even in full-wave rectification the ripple factor is quite high (0.482). Therefore, the rectified output is filtered to reduce its AC content.
- This is achieved by connecting a capacitor across the load as shown in figure below.
- Under steady conditions, when v_i is less than v_o, the capacitor feeds the load.
- When v_i increases above v_o the diode conducts till $v_o = v_c$ during which period the source charges the capacitor.
- The output waveform is as shown below, which has very much reduced ripple voltage.





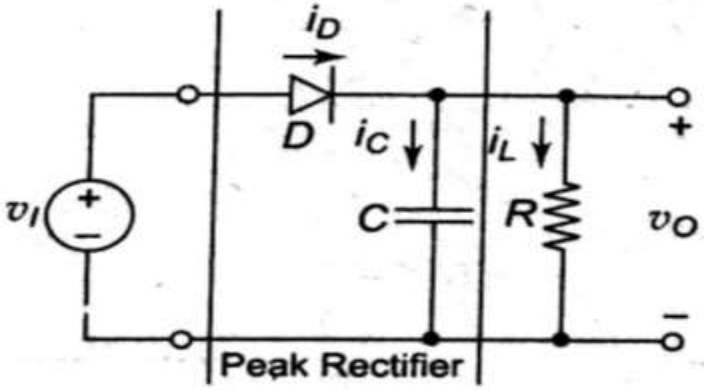
Choke Capacitor Filter:

- The choke capacitor filter is much more effective and is used for large DC power.
- The ripple factor can be made almost negligible because of the nonlinearity of choke not being used in low power electronic circuits. The figure is as shown below.

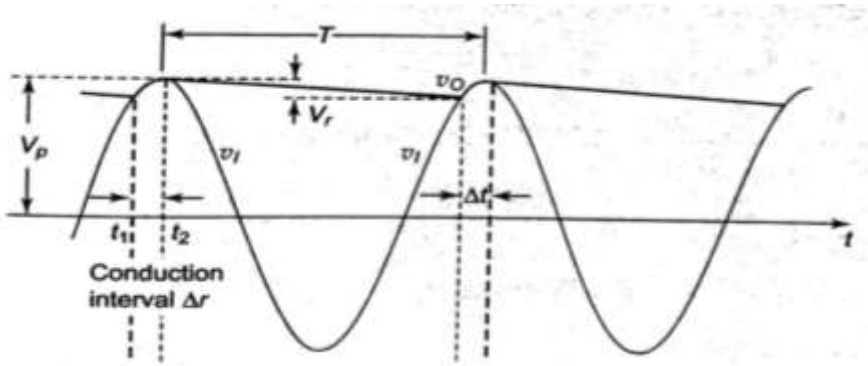


Peak Rectifier:

- Although, DC output can be attained in a rectifier but the performance of device is limited due to pulsating output. In order to improve the output and reduce the ripples, a capacitor filter is often used.
- In order to see the impact, let us consider a half-wave rectifier as shown in figure below. The capacitor C is added in parallel to load resistance R.
- The rectifier having the filter capacitor in parallel to diode is known as peak rectifier.

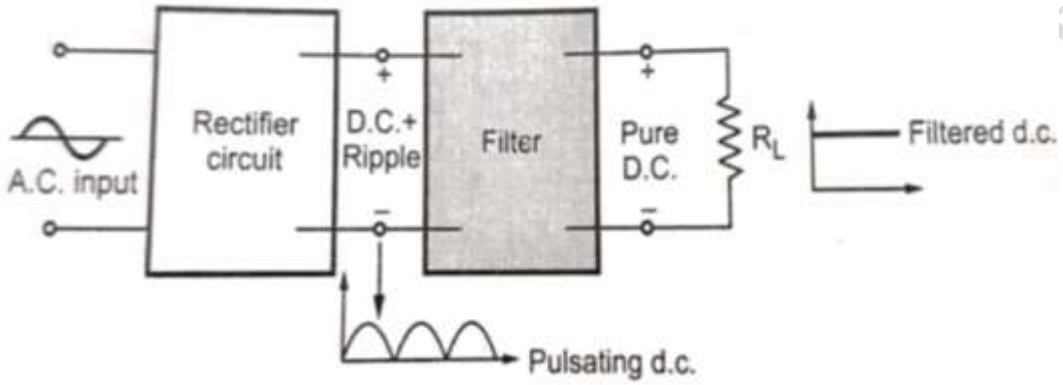


- In this case, capacitor charges during positive cycles of input voltage and discharges during the negative cycles.
- This impact is used to control the ripples across the output by controlling the discharging rate of capacitor; for this reason high value of C are used.
- The improvement in output is shown in below.

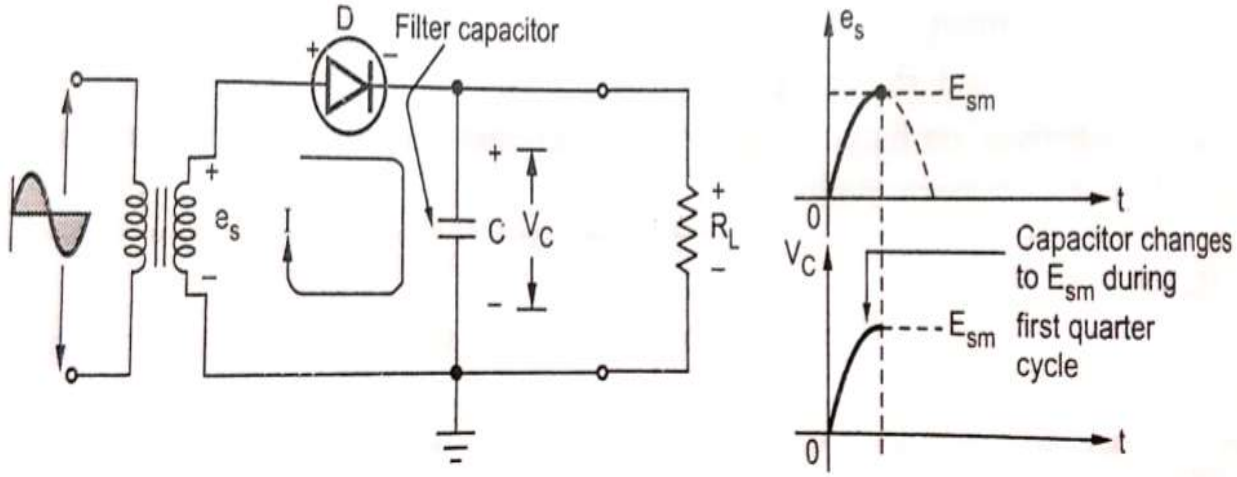


Filter Circuit:

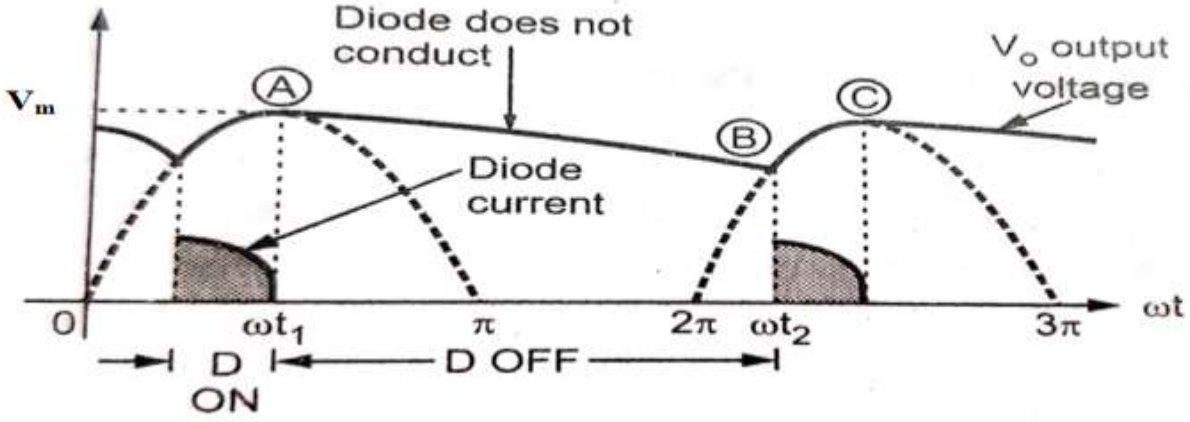
- The output of a half-wave and full-wave rectifier circuit is not pure DC which contains ripples.
- To minimize the ripple in the output, filters circuit are used.
- Filter circuits are connected between the rectifier and the load as shown in the figure.
- An AC input is applied to the rectifier circuit which produces the DC voltage output with ripple voltage.
- This will be fed as an input to the filter circuit which produces the pure DC by minimizing the ripple voltage.
- Usually capacitor is used as an filter element.



Half Wave Rectifier with capacitor filter:



- Figure above shows an half wave rectifier with capacitor input filter.
- Filter uses a single capacitor connected in parallel with the load.
- During the positive half cycle of the input, the diode is forward biased and this charges the capacitor C to the peak value of the input V_m.
- When input starts decreasing the peak value V_m, the capacitor remains charged at V_m and the diode gets reverse biased due to capacitor voltage.
- Hence during the complete negative half cycle and for some part of positive half cycle capacitor discharges through R_L as sown in the figure below.



- The voltage is same as the output voltage as it is in parallel with R_L.
- From the above figure it can be seen that diode conducts only from point **B** to **C** where capacitor gets charged to V_m. Thus diode gets forward biased.
- From point **A** to **B,** the diode remains non-conducting and conducts only for the period from **B** to **C**.
- Diode Current will be present for the period when diode is conducting.

Ripple Factor of Half wave Rectifier with filter:

- RMS value of output of capacitor filter circuit is given by:

$$\mathbf{V_{RMS}} = \frac{\boldsymbol{V_R}}{\mathbf{2\sqrt{3}}}$$

Where: V_R – Peak to Peak Ripple voltage

- During the time interval T_2 the capacitor C discharges through R_L. the charge discharged is given by:

$$\mathbf{Q = CV_R}$$

$$\mathbf{i} = \frac{\boldsymbol{dQ}}{\boldsymbol{dt}}$$

$$\mathbf{Q} = \int_0^{\boldsymbol{T_2}} \boldsymbol{i\, dt}$$

$$\mathbf{Q = I_{DC} * T_2}$$

- Average output or DC voltage is given by:

$$\mathbf{I_{DC} * T_2 = CV_R}$$

$$V_R = \frac{\boldsymbol{I_{DC} T_2}}{\boldsymbol{C}}$$

$\mathbf{T_2} = \mathbf{T}$ since $\mathbf{T_1}+\mathbf{T_2} = \mathbf{T}$ and $T_1 \gg T_2$ and $T = 1 / f$

$$V_R = \frac{\boldsymbol{I_{DC}\, T}}{\boldsymbol{C}}$$

$$V_R = \frac{\boldsymbol{I_{DC}}}{\boldsymbol{fC}}$$

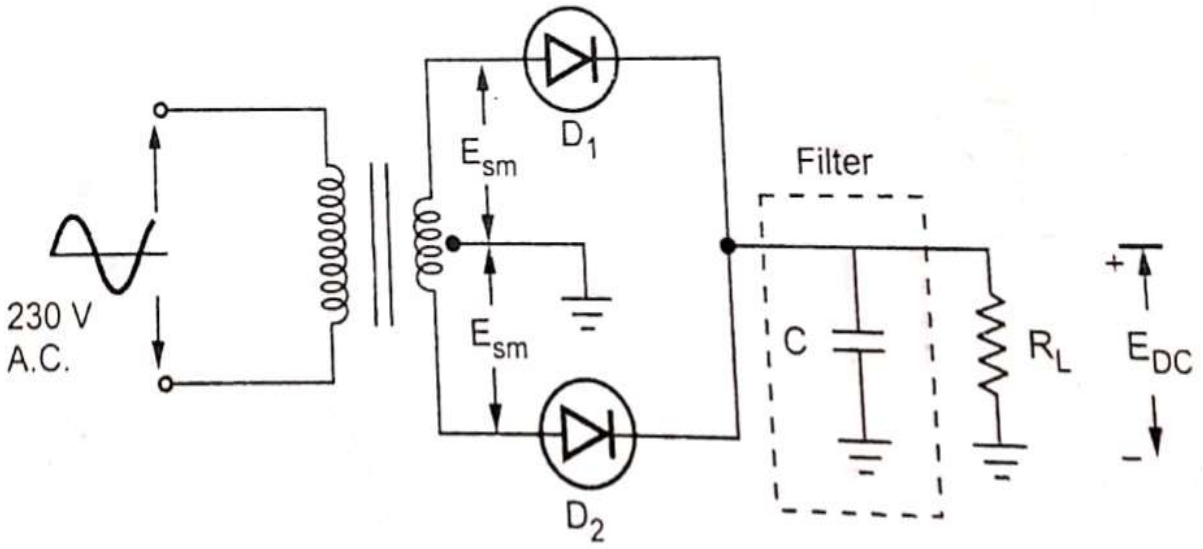
$$I_{DC} = \frac{\boldsymbol{V_{DC}}}{\boldsymbol{R_L}}$$

$V_R = \frac{V_{DC}}{fCR_L}$ peak to peak Ripple Voltage

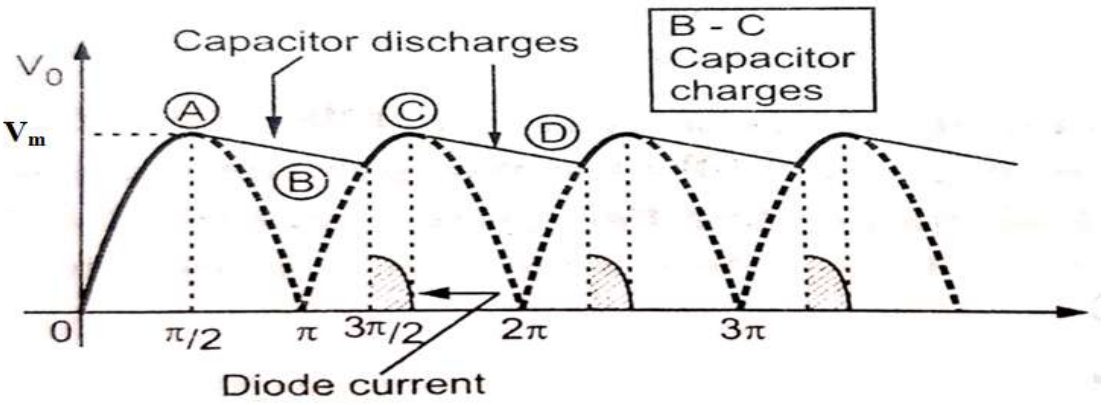
$$\textbf{Ripple Factor} = \frac{V_{RMS}}{V_{DC}} = \frac{\frac{V_R}{2\sqrt{3}}}{V_{DC}} = \frac{V_{DC}}{V_{DC}\,2\sqrt{3}\,fCR_L}$$

$$\textbf{Ripple Factor} = \frac{1}{2\sqrt{3}\,fCR_L} \textbf{ for Half Wave Rectifier}$$

Full Wave Rectifier with capacitor filter:

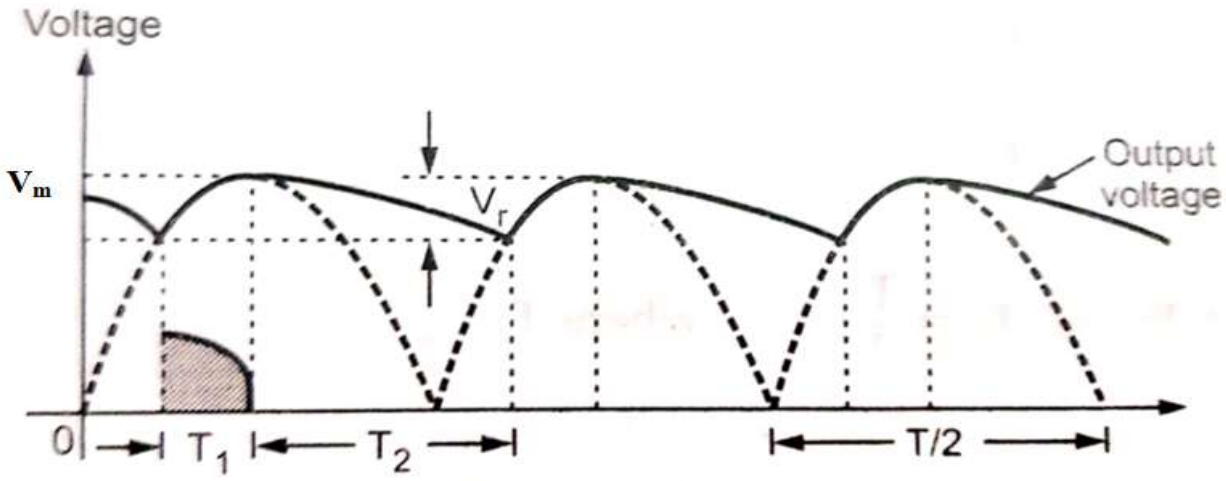


- Figure above shows an half wave rectifier with capacitor input filter.
- Filter uses a single capacitor connected in parallel with the load.
- During the positive half cycle of the input, the diode **D_1** is forward biased and this charges the capacitor C to the peak value of the input V_m.
- Once the diode is charged to V_m, the diode **D_1** becomes reverse bias and stops conducting and capacitor discharges until **B**.
- Once the capacitor gets the threshold value, capacitor gets charged to peak value V_m i.e. from **B** to **C.**



- During time T_1, capacitor gets charged and this process is quick.
- During time T_2, capacitor gets discharged through $\mathbf{R_L}$ slowly and hence $T_1 \gg T_2$
- Diode Current will be present for the period when diode is conducting.

Ripple Factor of Full wave Rectifier with filter:



- RMS value of output of capacitor filter circuit is given by:

$$\mathbf{V_{RMS}} = \frac{\boldsymbol{V_R}}{\mathbf{2\sqrt{3}}}$$

Where: V_R – Peak to Peak Ripple voltage

- During the time interval T_2 the capacitor C discharges through R_L. the charge discharged is given by:

$$\mathbf{Q = CV_R}$$

$$\mathbf{i} = \frac{\boldsymbol{dQ}}{\boldsymbol{dt}}$$

$$\mathbf{Q} = \int_0^{\boldsymbol{T_2}} \boldsymbol{i\, dt}$$

$$\mathbf{Q = I_{DC} * T_2}$$

- Average output or DC voltage is given by:

$$\mathbf{I_{DC} * T_2 = CV_R}$$

$$\mathbf{V_R} = \frac{\boldsymbol{I_{DC} T_2}}{\boldsymbol{C}}$$

$\mathbf{T_2} = \mathbf{T}$ since $\mathbf{T_1 + T_2} = \frac{\boldsymbol{T}}{\mathbf{2}}$ and $T_1 \gg T_2$ and $T = 1 / f$

$$V_R = \frac{\boldsymbol{I_{DC}\, T}}{\boldsymbol{2C}}$$

$$V_R = \frac{\boldsymbol{I_{DC}}}{\boldsymbol{2fC}}$$

$$I_{DC} = \frac{\boldsymbol{V_{DC}}}{\boldsymbol{R_L}}$$

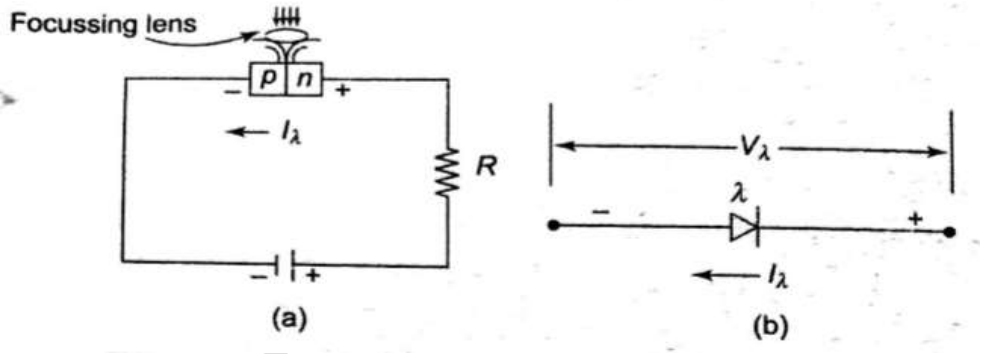
$V_R = \frac{V_{DC}}{2fCR_L}$ peak to peak Ripple Voltage

$$\textbf{Ripple Factor} = \frac{V_{RMS}}{V_{DC}} = \frac{\frac{V_R}{2\sqrt{3}}}{V_{DC}} = \frac{V_{DC}}{V_{DC}\, 4\sqrt{3} fCR_L}$$

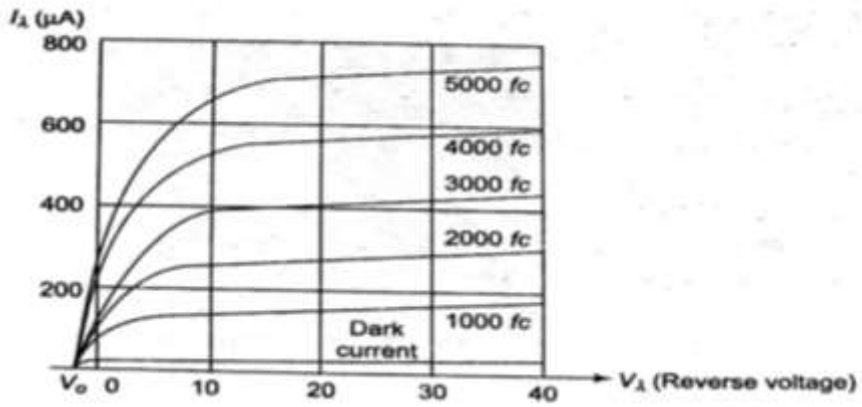
$$\textbf{Ripple Factor} = \frac{1}{4\sqrt{3} fCR_L} \quad \textbf{for Full Wave Rectifier}$$

Photo Diode:

- Photodiode is a semiconductor PN-junction device whose region of operation is limited to the reverse bias region.
- The biasing arrangement, construction and symbol for the device is as follows:



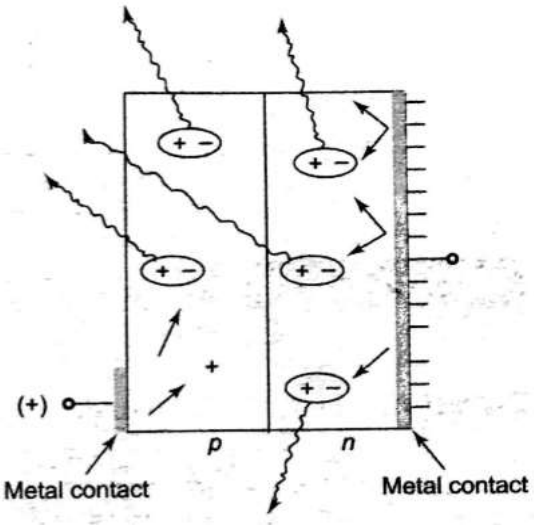
- Reverse saturation current is normally limited to a few micro amperes.
- The application of light to the junction will result in a transfer of energy from the incident travelling light waves to the atomic structure, resulting in an increased number of minority carriers and an increased level of reverse current.
- That is shown in below figure for different intensity levels,



- "Dark current is the current that will exist with no applied illumination".

Light Emitting Diode [LED]:

- In a forward bias PN-junction, diode recombination of electrons and holes takes places at the junction and within the body of the crystal, particularly at the location of a crystal defect.
- Upon capture of a free electron by a hole, the electron goes into a new state and its kinetic energy is given off as heat and as light photons.
- In a silicon diode, most of this energy is given off as heat but in other materials such as Gallium Arsenide (GaAs) or Gallium Phosphide (GaP), sufficient numbers of photons (light) are generated so as to create a visible source.
- This process of light emission in PN-junction of such materials is illustrated in the figure below and is known as ***Electroluminescence***.
- The metal contact of P-material is made much small to permit the emergence of maximum number of photons so that in an LED, the light lumens generated per watt of electric power is quite high.
- Intensity of light increases almost linearly with forward current, depending on the material used.
- The voltage levels of LEDs are 1.7V to 3.3V which is compatible with the solid state circuits.
- LEDs have short response time and light contrast is good.
- LEDs emit light red, green, orange or blue.

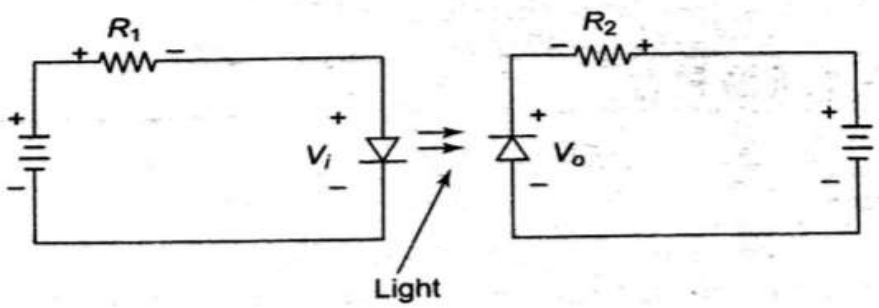


Applications:

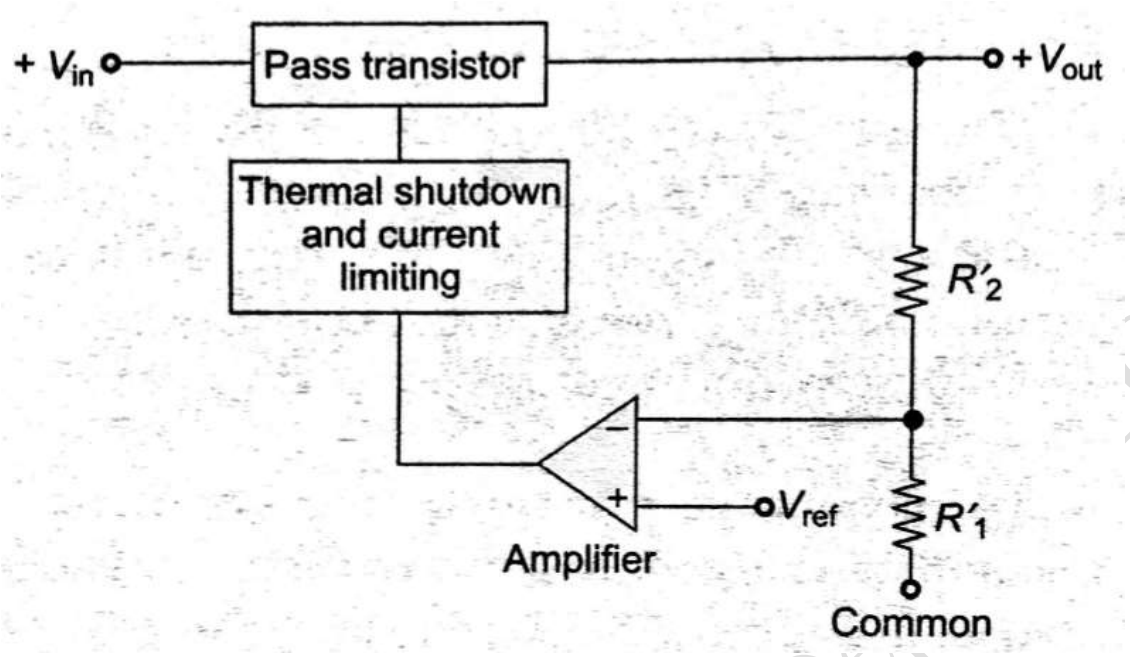
LEDs find several display applications, particularly in 8-segment display of numbers 0 to 9, also in LED TV's.

Photocoupler:

- It is a package of an LED and photodiode whereas circuits are electrically isolated as shown in figure below.
- The LED is forward biased and the photodiode is reverse biased. The output is available across R_2.



LM 78XX Series:



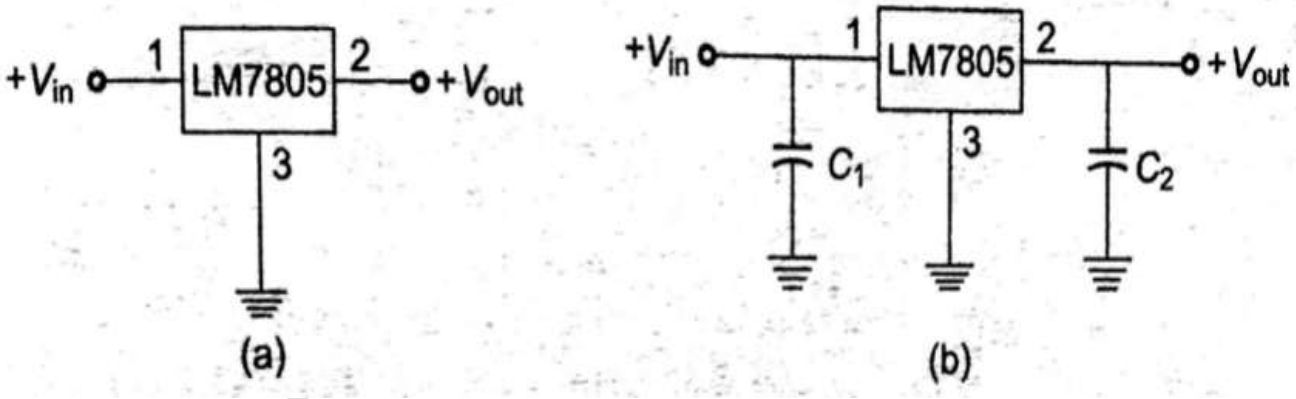
- The LM 78XX series [where XX= 05,06,08,10,12,15,18 or 24] is typical of the three terminal voltage regulators.
- The 7805 produces an output of +5V, the LM7806 produces +6V and so on upto 7824, which produces an output of +24V.
- The figure below shows the functional block diagram for the 78XX series.
- A built-in reference voltage V_{ref} drives the non-inverting input of an amplifier.
- A voltage divider consisting of $R`_1$ and $R`_2$ samples the output voltage and returns a feedback voltage to the inverting input of a high-gain amplifier.
- The output voltage is given by

$$\boldsymbol{V_{out} = \frac{R`_1 + R`_2}{R`_1} * V_{ref}}$$

- The circuit with resistors are built inside the IC.
- The LM78XX includes a pass transistor that can handle 1A of load current.
- The tolerance of the output voltage is ±4 %.
- These IC can withstand upto maximum of 175^o.

Fixed Voltage Regulator LM7805:

- Figure below shows an LM7805 connected as a fixed voltage regulator.
- Pin 1 is the input, Pin 2 is the output and Pin 3 is ground.
- The LM7805 has an output voltage of +5V and a maximum load current over 1A.
- The typical load regulation is 10mV for a Load current between 5mA and 1.5A.
- The typical line regulation is 3mV for an input voltage of 7 to 25V.
- It also has a ripple rejection of 80dB.
- A bypass capacitor C_1 is used at Pin 1 to reduce the input oscillations inside the IC.
- To improve the transient response of the regulated output voltage, a bypass capacitor C_2 is connected at Pin 2.
- Any regulations in the 78XX series has a drop-out voltage of 2V to 3V, depends on the output voltage.
- Hence the input voltage must be atleast 2V to 3V more than the output voltage.
- LM7805 will regulate over an input range of approximately 8 to 20V.



MODULE 2

FET CHARACTERSTICS AND SCR

Introduction to FET:

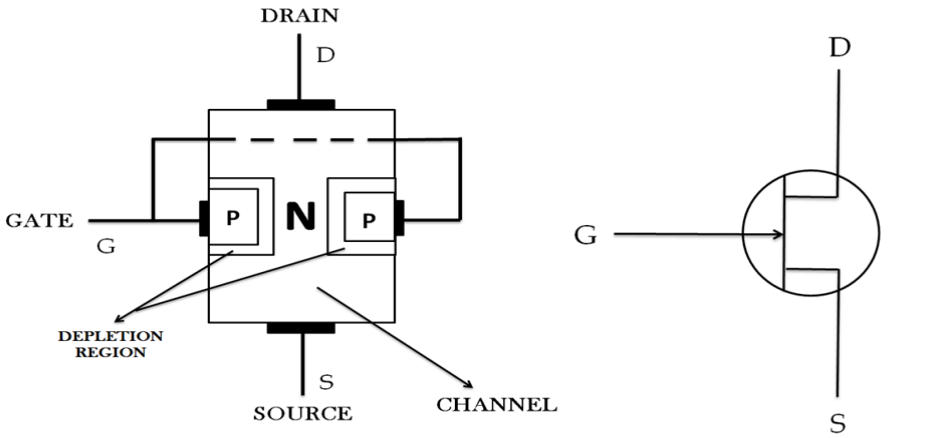
- FET is the abbreviation of **Filed Effect Transistor**.
- FET's are **unipolar** devices.
- FET's are semiconductor device, which has three terminals named as Source(S), Drain(D) and Gate(G), which are used as Amplifiers or Switches.
- Gate terminal acts as controlling terminal, i.e. the voltage applied between the gate and the source terminal control the output drain current I_D. Hence FET's are called as **Voltage Controlled Devices.**
- FET's are categorised as:
    1. Junction Field Effect Transistors [JFET].
    2. Metal Oxide Semiconductor Field Effect Transistor [MOSFET].
    3. Metal Semiconductor Field Effect Transistors [MESFET].

Junction Field Effect Transistor:

N-channel JFET:

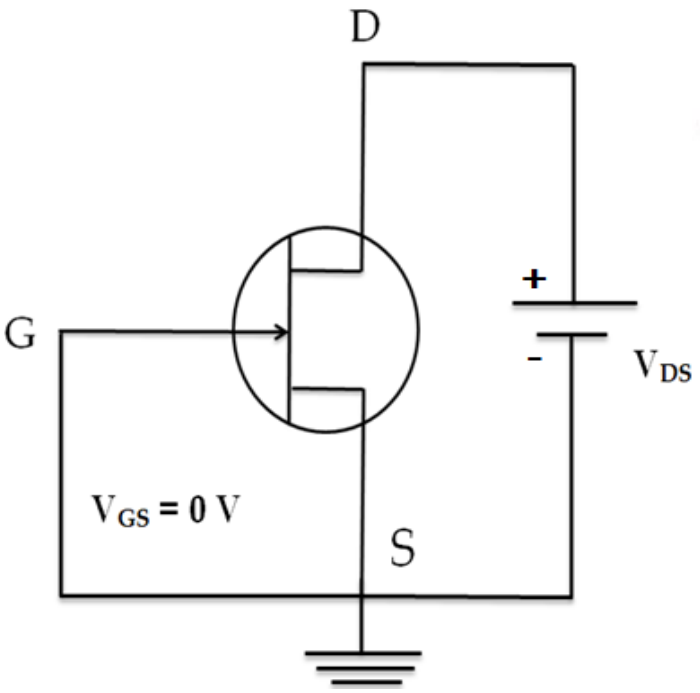
Construction:

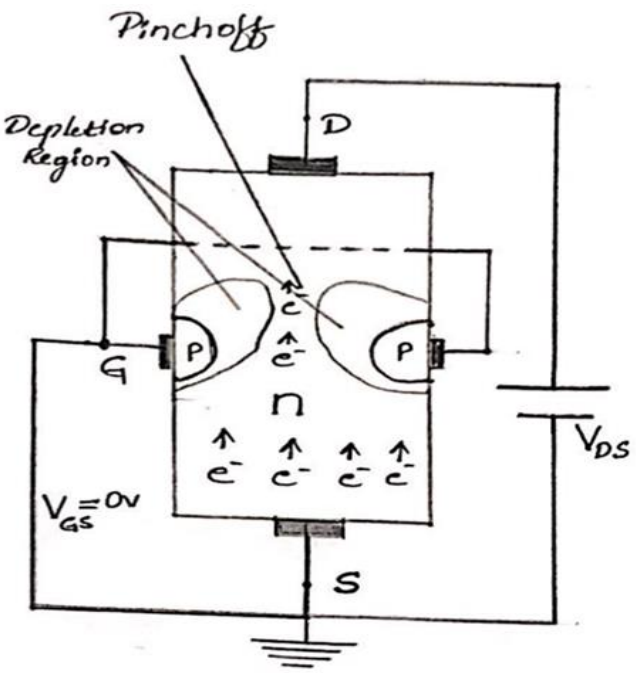
- In an n-channel JFET, an N-type semiconductor material forms a channel between embedded layers of P-type material.
- Hence two P-N junctions are formed between the semiconductor channel and the embedded semiconductor layers.
- Ohmic contacts or Metal contacts are placed at the top and bottom of the channel and are referred to as the Drain (D) and the Source(S) terminals.
- The channel behaves as an resistive element between drain and source terminal.
- In an N-channel JFET, both the embedded P-type layers are connected together and form the GATE(G) terminal.
- Figure below shows the cross section of N-Channel JFET with its symbolic representation.



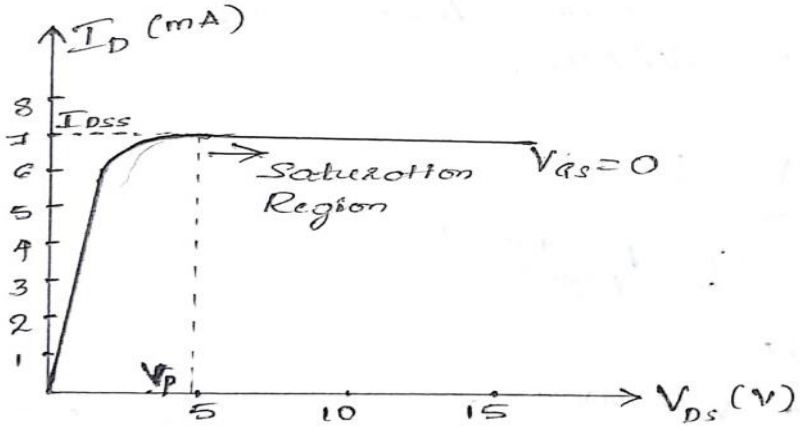
SYMBOLIC REPRESENTATION

Operation and Characteristics:

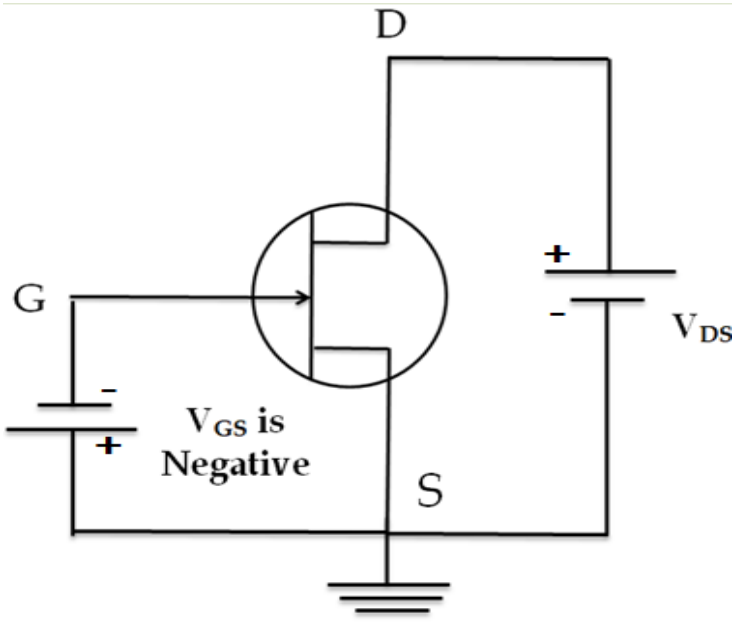




- Let us consider N-channel JFET, to which a ***positive drain-source voltage (V_{DS})*** is applied with gate terminal shorted to the source terminal ***(V_{GS} = 0)***.
- When the positive drain source voltage is applied, the ***electrons in the N-channel are attracted to the drain terminal establishing flow of drain current I_D,*** whose value is determined by the value of the applied V_{DS} and the resistance of the N-channel between the drain and the source terminal.
- Due to the flow of I_D, there will be uniform voltage drop above the channel resistance which reverse bias the Two PN junction which results in increasing the width of the depletion region.
- ***I_D increases with increase in the V_{DS}*** till the V_{DS} reach a point of saturation. ***The value of the V_{DS} where the I_D gets saturated*** is referred to as the ***Pinch-Off voltage (V_P)***.
- When ***V_{DS} reaches V_P,*** the value of I_D doesn't changes with further increase in the value of V_{DS} which is called as Pinch off condition.
- Therefore I_D essentially remains constant for $\mathbf{V_{DS} > V_P}$.
- This current is called as Drain to Source current for short circuit connection between gate and source [I_{DSS}].



- In n-channel JFET, the voltage V_{GS} is negative, that's the gate terminal is made more negative than the source terminal.
- When a negative voltage is applied to the gate terminal, there is increase in the width of depletion region. As the value of $\mathbf{V_{GS}}$ becomes more negative, the value of saturation current decreases further and drain current becomes zero for $\mathbf{V_{GS}}$ equal to $\mathbf{-V_P}$.



- The left region of the locus of the pinch-off voltage is the Ohmic region or the voltage controlled region. In Ohmic region, JFET acts as a variable resistor, whose resistance is controlled by the applied gate-source voltage.
- Region to the right of the locus of the pinch-off voltage is the saturation region.

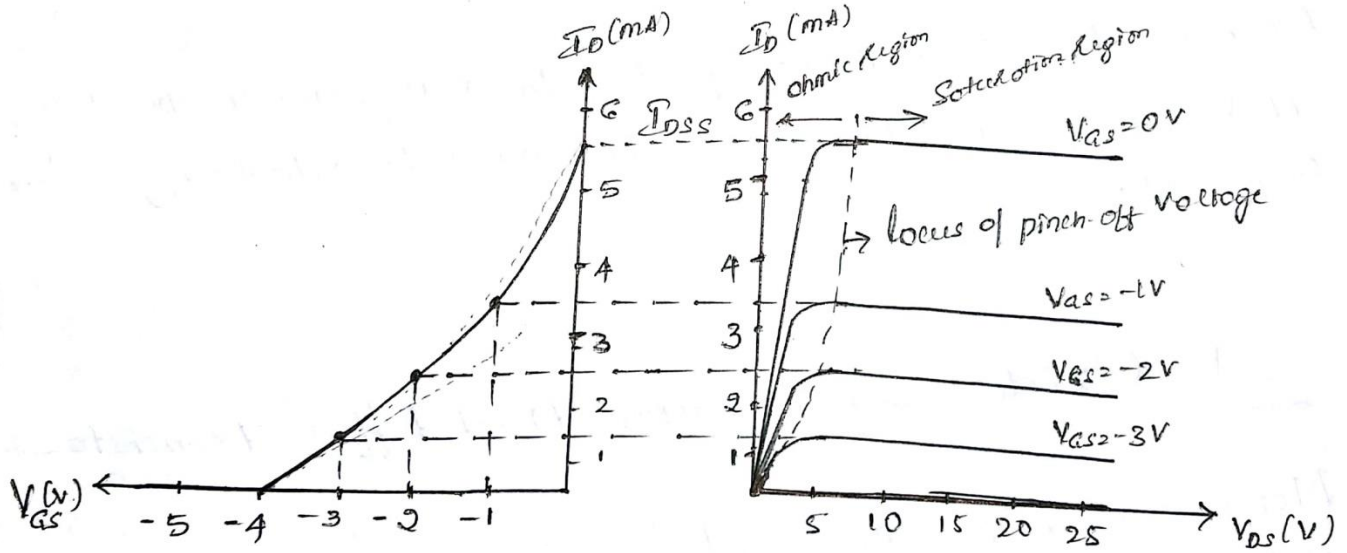
- Drain resistance in the saturation region is given by;

$$r_d = \frac{r_o}{(1 - \frac{V_{GS}}{V_P})^2}$$

- Relationship between the output current I_D in the saturation region for the given value of input voltage V_{GS} is given by the below equation which is called as Shockley's equation;

$$\mathbf{I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2}$$

- Drain characteristics of the JFET is plotted between $\mathbf{I_D}$ and $\mathbf{V_{DS}}$ for $\mathbf{V_{GS} = 0\ V}$.
- Transfer characteristics are plotted between $\mathbf{I_D}$ and $\mathbf{V_{GS}}$, which can also be plotted using Shockley's equation.
- Characteristic curve is plotted between $\mathbf{I_D}$ and $\mathbf{V_{DS}}$ for different values of $\mathbf{V_{GS}}$.
- The transfer characteristic curve and the output/total characteristic curve is as shown below.



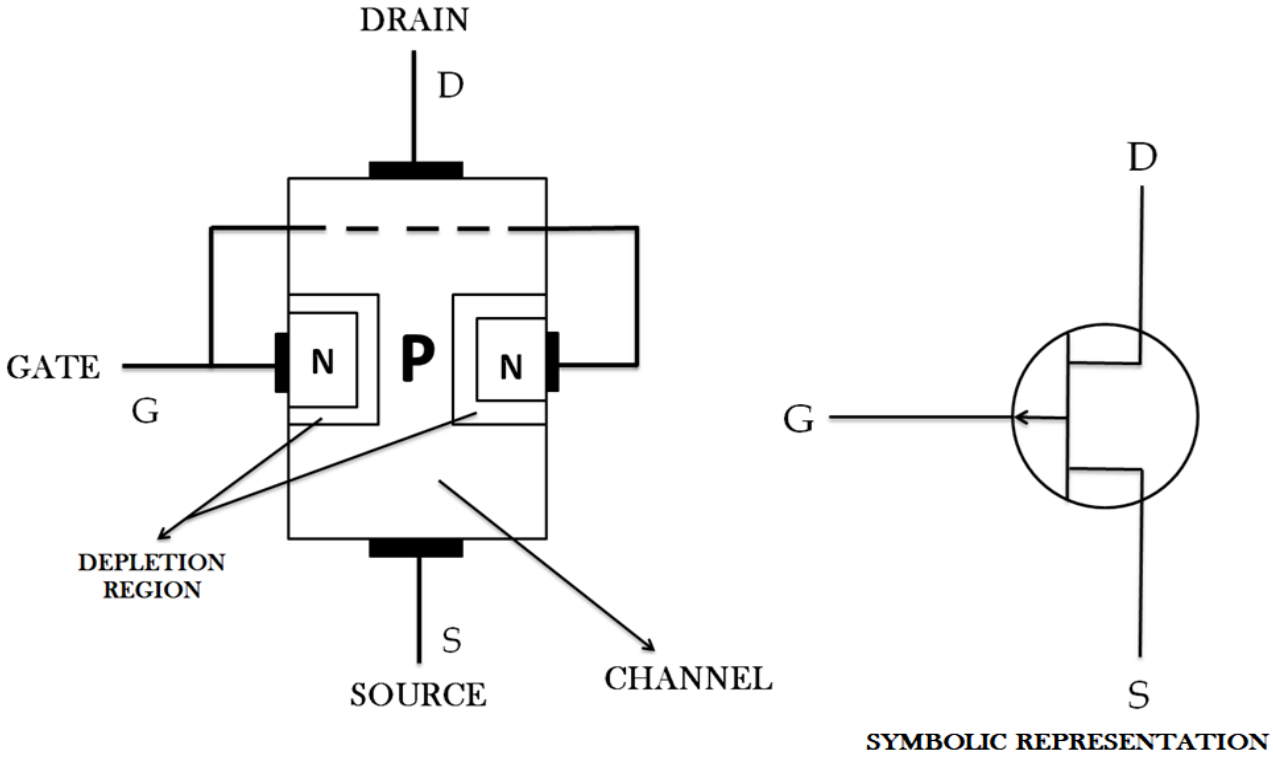
TRANSFER CHARACTERISTIC CURVE

OUTPUT CHARACTERISTIC CURVE

P-Channel JFET

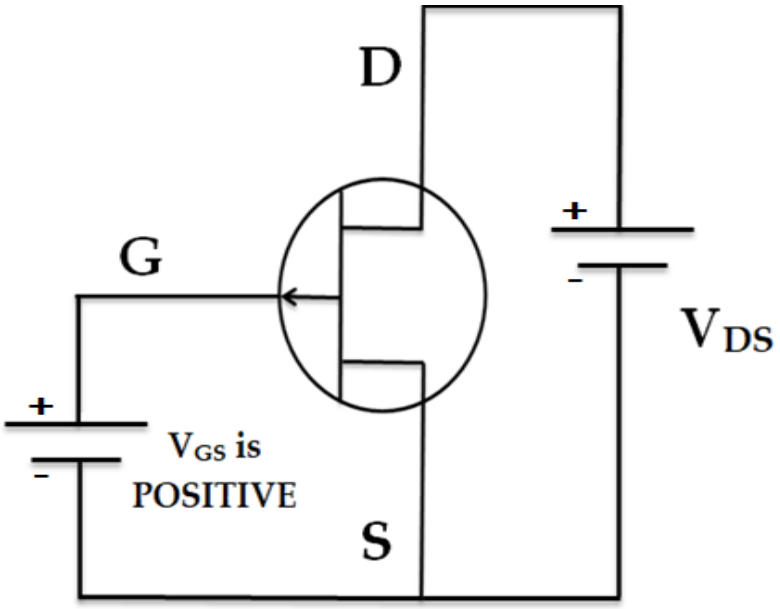
Construction:

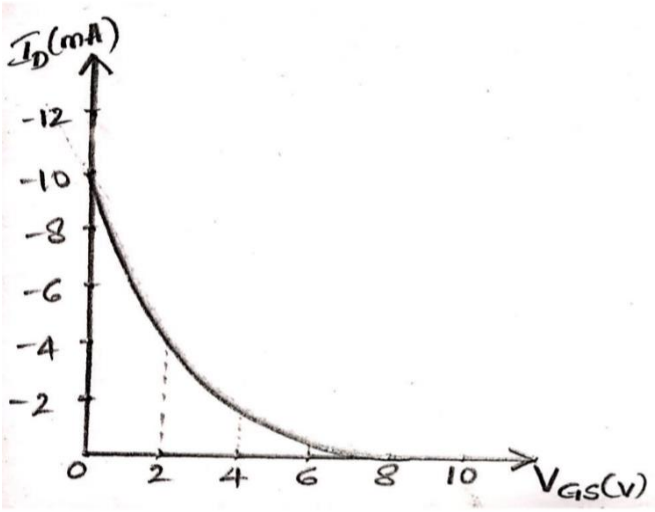
- In an p-channel JFET, an p-type semiconductor material forms a channel between embedded layers of n-type material.
- Hence two P-N junctions are formed between the semiconductor channel and the embedded semiconductor layers.
- Ohmic contacts or Metal contacts are placed at the top and bottom of the channel and are referred to as the Drain(D) and the Source(S) terminals.
- The channel behaves as a resistive element between drain and source terminal.
- In an P-channel JFET, both the embedded N-type layers are connected together and form the GATE(G) terminal.
- Figure below shows the cross section of P-Channel JFET with its symbolic representation.



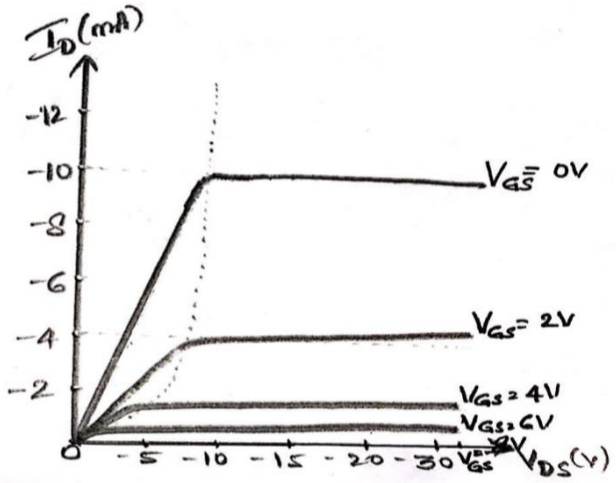
Operation:

- A voltage source is connected between Drain and Source terminals **(V_{DS})** making drain negative and source positive. Gate and Source terminals are shorted **($V_{GS} = 0$)**.
- The region between the two doped n-substrate acts as channel.
- Electrons attracts holes inducing **Negative Drain Current (I_D)** which gets increases linearly with the increase of V_{DS} and gets saturated for further increasing of V_{DS}.
- A voltage source is connected between Gate and Source terminal **(V_{GS})** making gate positive and source negative.
- By applying positive gate to source voltage **(V_{GS})**, it controls the flow of I_D as shown in the characteristic curve.
- At $V_{GS} = -V_P$, I_D becomes zero.
- The characteristic curve is shown below.





TRANSFER CHARACTERISTIC CURVE



TOTAL/OUTPUT CHARACTERISTIC CURVE

MOSFET:

- Metal Oxide FET is insulated from the semiconductor channel by a very thin oxide layer.
- MOSFET's are classified into two types, depending on their construction and mode of operation;
  1. Depletion Type MOSFET [DE-MOSFET]
  2. Enhancement Type MOSFET [E - MOSFET]

Depletion MOSFET:

"The device which conducts under zero gate bias are called or zero gate voltage are called Depletion MOSFET".

In this type, there is a physical channel present between Source and Drain terminal.

Enhancement MOSFET:

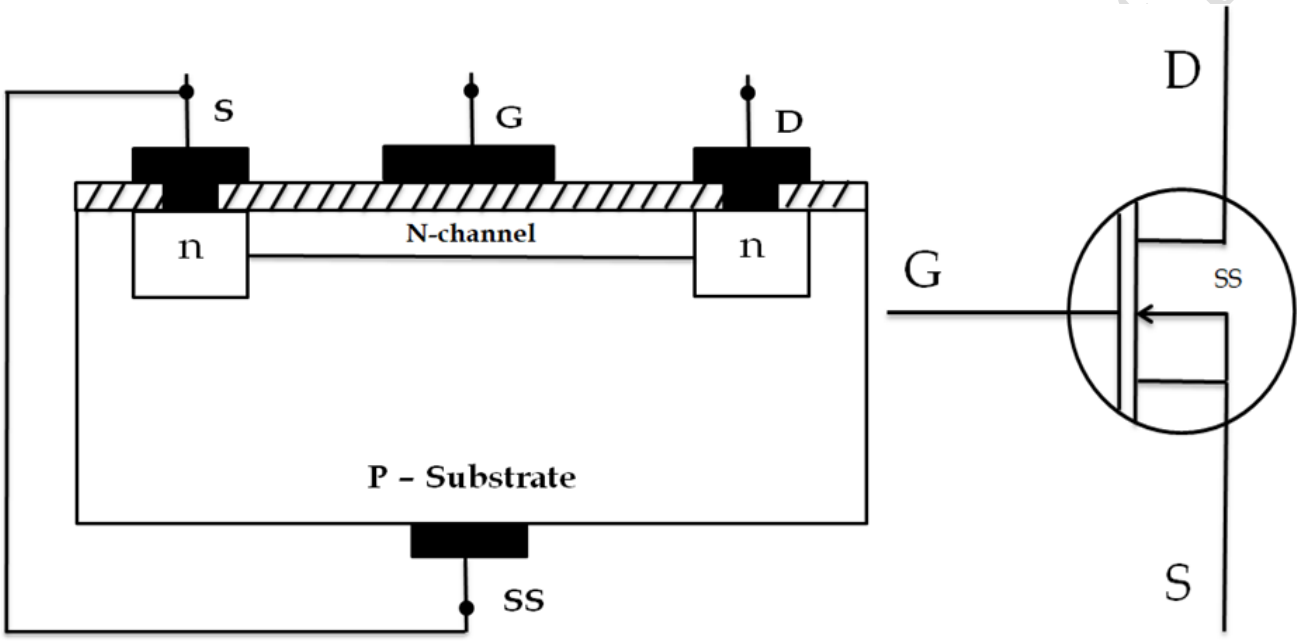
"The device which do not conducts under zero gate bias are called or zero gate voltage are called Depletion MOSFET".

In this type, there is no physical channel between Source and Drain terminal.

N-channel Depletion Type MOSFET:

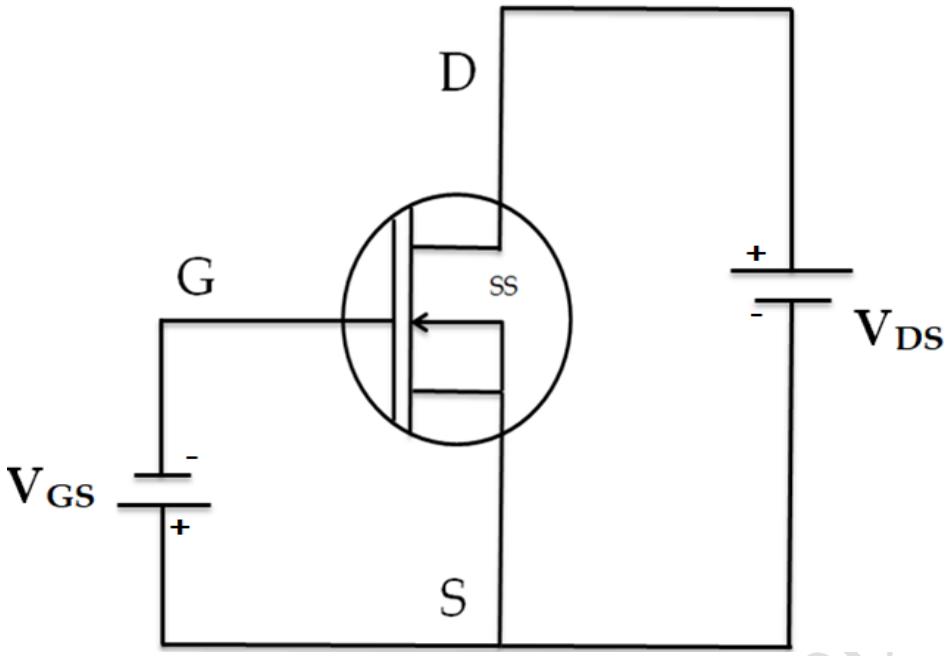
Construction:

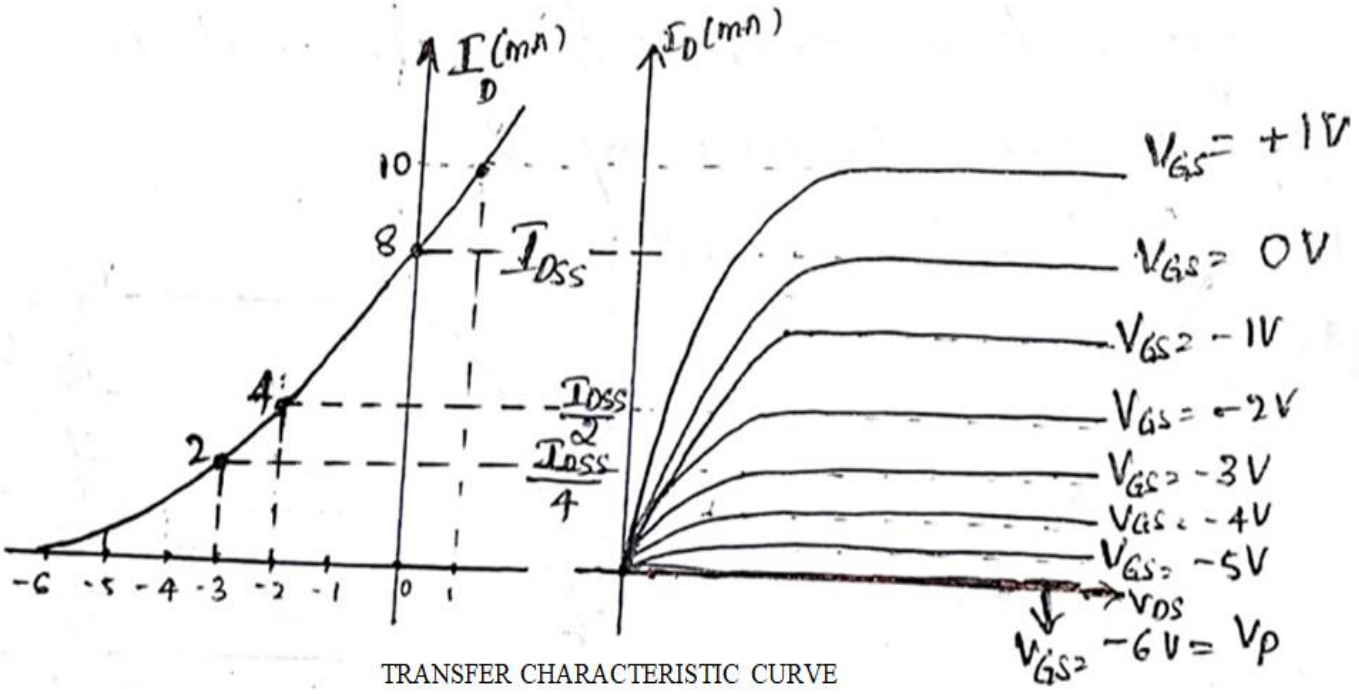
- Consider a slab of P-type substrate which is attached with a metallic contact called as Substrate terminal(SS).
- Two N-type materials are doped in the p-type substrate which is connected through the metallic contacts, which forms the two terminals namely Source(S) and Drain(D).
- Between these two N-type regions, an N channel is formed on the P-type substrate which acts as a gate terminal. But a very thin silicon oxide[SiO_2] layer separates the metal of the gate terminal from the channel.
- The N-channel Depletion type MOSFET is as shown below with its symbolic representation.



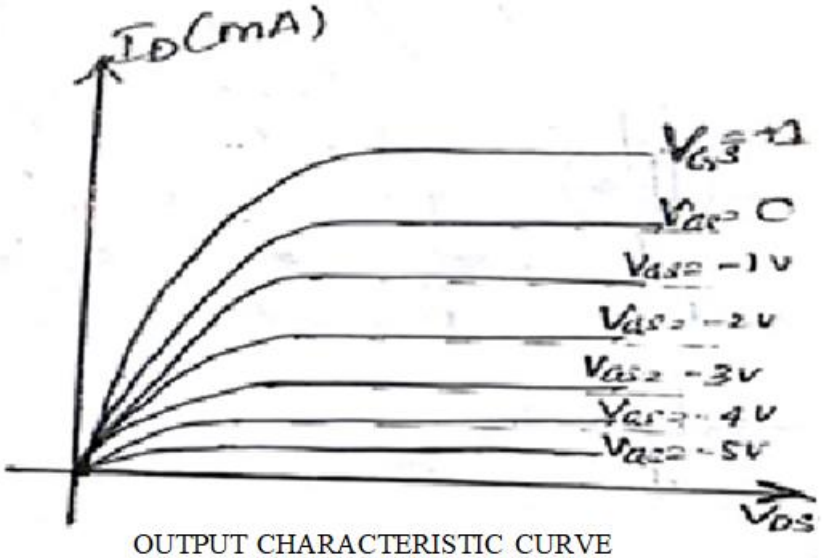
Operation:

- First the gate to source voltage is set 0 volts ($\mathbf{V_{GS} = 0}$) by the direct connection from one terminal to other. [i.e. shorted].
- Voltage $\mathbf{V_{DS}}$ is applied across the drain to source terminal which makes drain more positive than source.
- By making drain more positive, the positive potential at the drain attracts the electrons from the source through the n channel which induces the **Drain Current $\mathbf{I_D}$**.
- The resulting current at $\mathbf{V_{GS} = 0V}$ is labelled as $\mathbf{I_{DSS}}$.
- When the gate terminal is at negative potential as compared to the source terminal, electrons in the N-channel are repelled by this negative potential towards the P-type substrate and also the holes in the P-type substrate are attracted towards the gate and recombination takes place results in reduction of free electrons in the N-channel.
- Higher the negative potential, more is the recombination and less the number of free electrons in the channel. Hence the drain current decreases with increase in the value of negative gate-source potential.
- The region for zero and negative value of gate-source voltage is referred to as the Depletion region.
- Figure below shows the circuit connection of biasing of N-channel DE MOSFET and the transfer characteristics and output characteristics.





TRANSFER CHARACTERISTIC CURVE

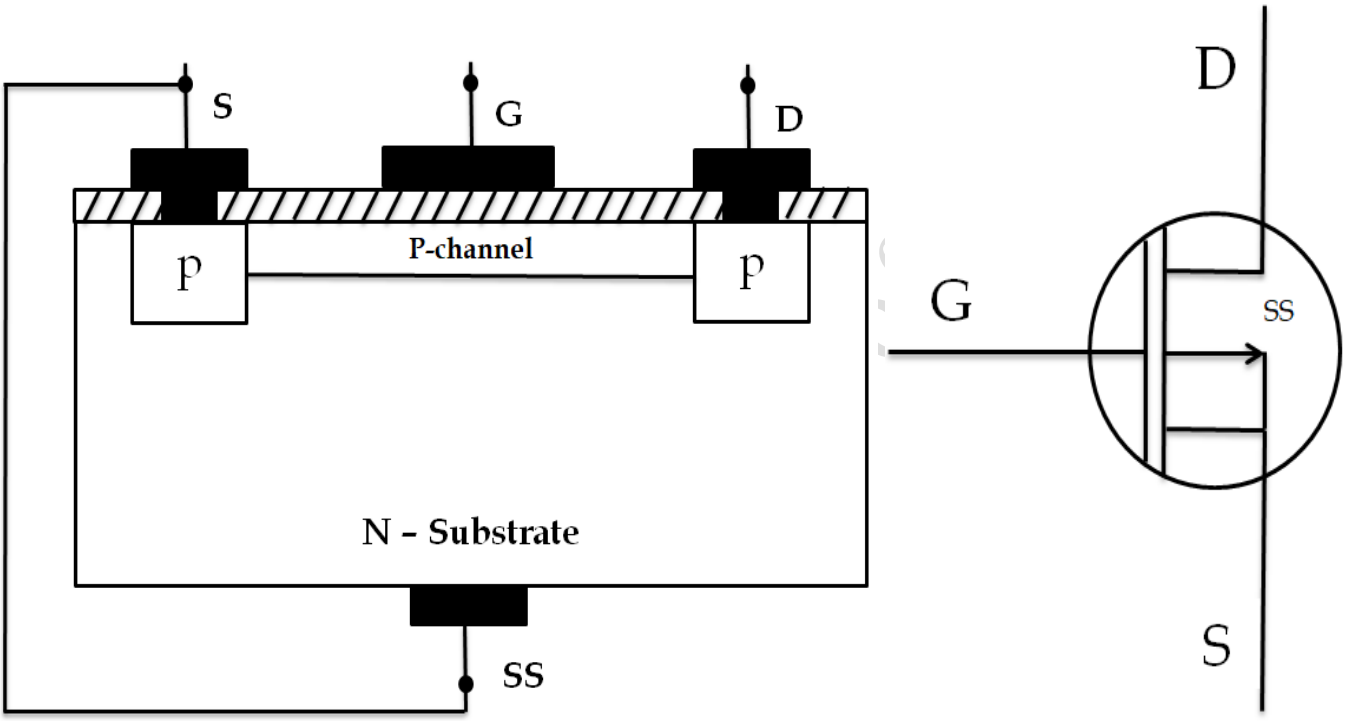


OUTPUT CHARACTERISTIC CURVE

P-channel Depletion Type MOSFET:

Construction:

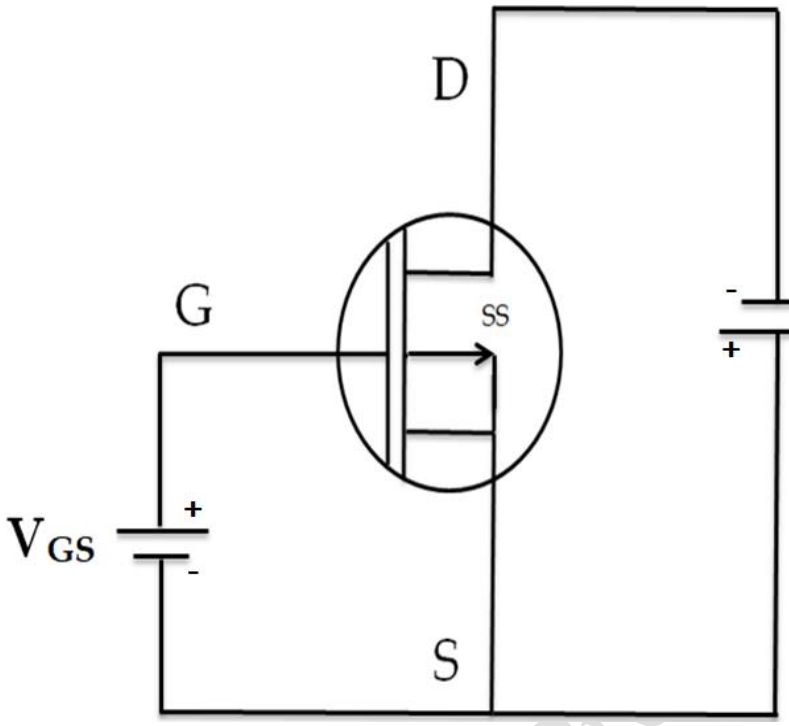
- Consider a slab of P-type substrate which is attached with a metallic contact called as Substrate terminal (SS).
- Two N-type materials are doped in the p-type substrate which is connected through the metallic contacts, which forms the two terminals namely Source(S) and Drain(D).
- Between these two N-type regions, an N channel is formed in the P-type substrate which acts as a gate terminal. But a very thin silicon oxide **[SiO_2]** layer separates the metal of the gate terminal from the channel.
- The N-channel Depletion type MOSFET is as shown below with its symbolic representation.

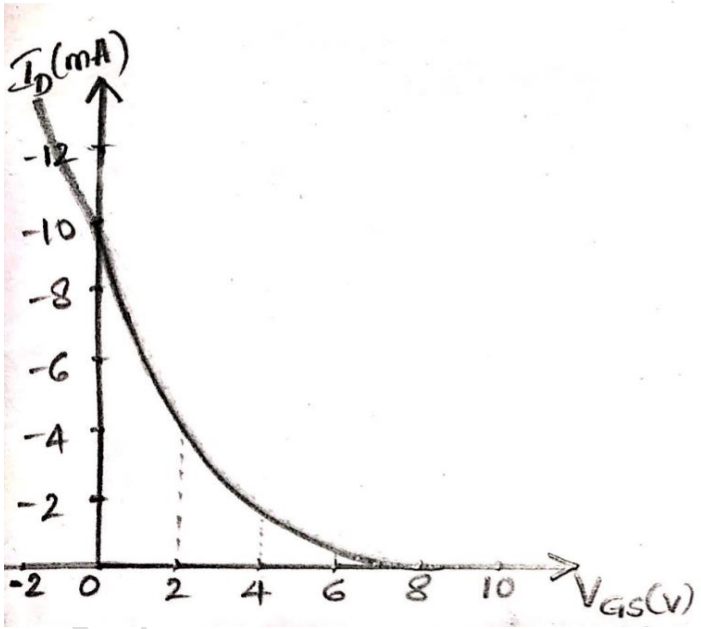


Operation:

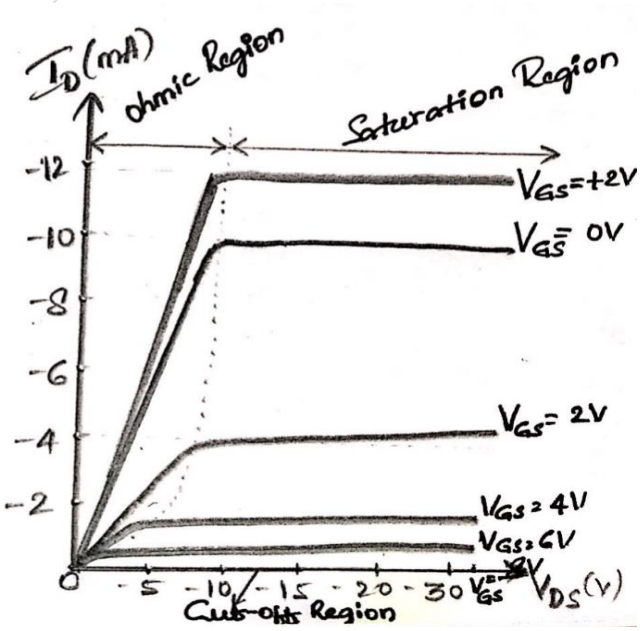
- The gate to source voltage is set 0 volts **($V_{GS} = 0$)** by the direct connection from one terminal to other. [i.e. shorted].
- A voltage source is connected between drain and source terminal making drain negative and source positive **(V_{DS})**.
- By making drain more negative, the negative potential at the drain attracts the holes from the source through the p-channel which induces the **Negative Drain Current I_D**. The resulting current at **$V_{GS} = 0V$** is labelled as **I_{DSS}**.
- When the gate terminal is at positive potential as compared to the source terminal, **holes** in the P-channel are repelled by this positive potential towards the N-type substrate and also the electrons in the N-type substrate are attracted towards the gate and recombination takes place results in reduction of free holes in the P-channel.
- Higher the positive potential, more is the recombination and less the number of free holes in the channel. Hence the drain current decreases with increase in the value of positive gate-source potential.

- The region for zero and positive value of gate-source voltage is referred to as the Depletion region.
- Figure below shows the circuit connection of biasing of P-channel DE MOSFET and the transfer characteristics and output characteristics.





TRANSFER CHARACTERISTIC CURVE



TOTAL/OUTPUT CHARACTERISTIC CURVE

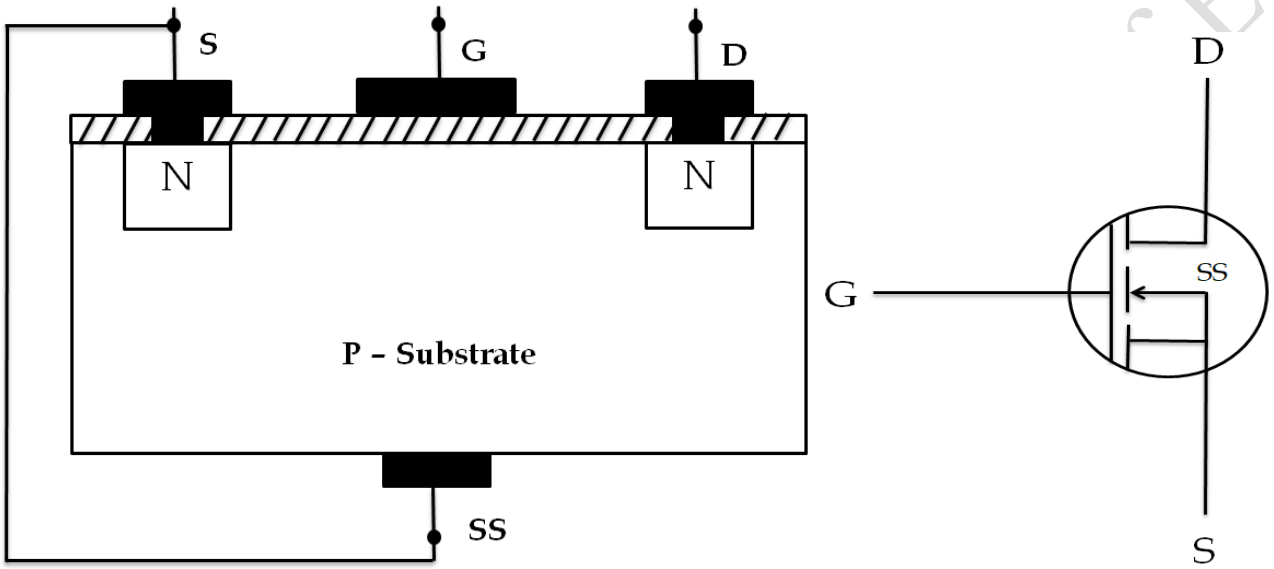
Enhancement MOSFET:

- Here the physical channel is not present.
- Drain current will be cut-off until the gate-to-source **[V_{GS}]** voltage reaches a specific magnitude.

N-channel Enhancement Type MOSFET:

Construction:

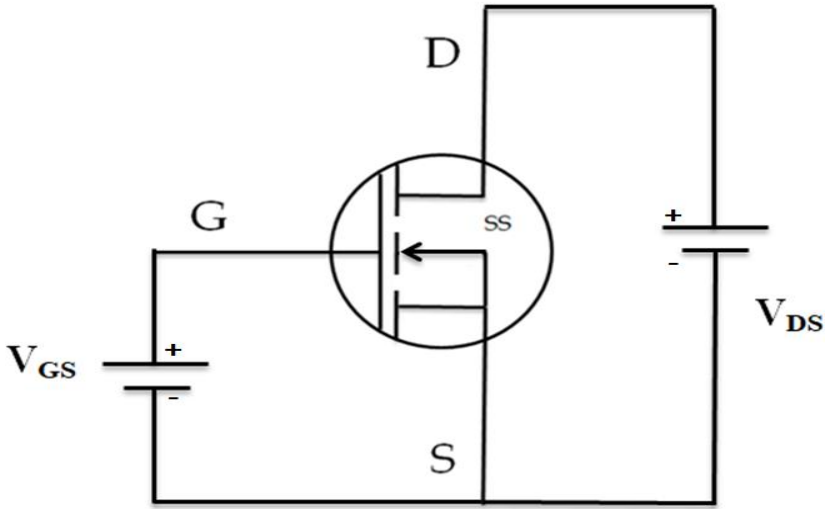
- Consider a slab of P-type substrate which is attached with a metallic contact called as Substrate terminal(SS).
- Two N-type materials are doped in the p-type substrate which is connected through the metallic contacts, which forms the two terminals namely Source(S) and Drain(D).
- Here there is no physical cannel between the source and the drain terminals.
- The n-channel E-MOSFET is as shown in the figure below;
- Dotted lines in the symbolic representation individuals the absence of channel.

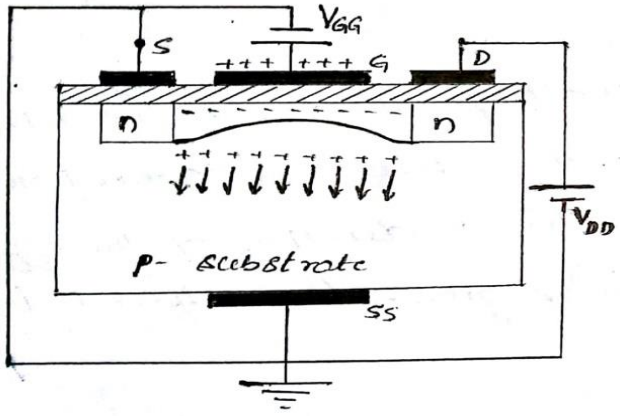


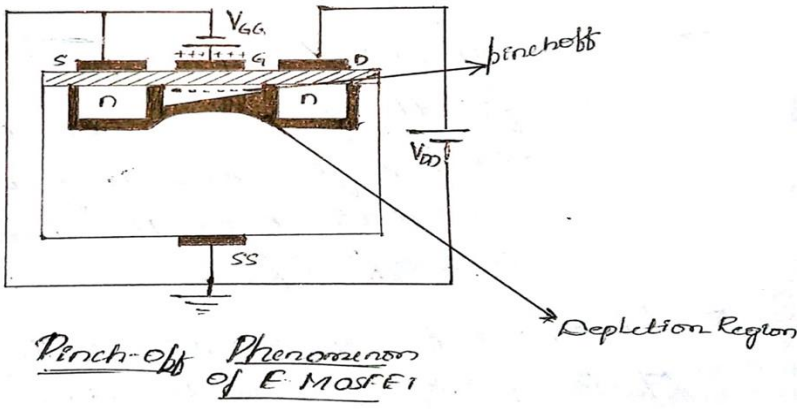
Operation:

- When the gate-to-source voltage $\mathbf{V_{GS}}$ is zero and a voltage is applied between the drain and the source V_{DS} in the absence of n-channel will result in a current of effectively 0A.
- Drain current flows only when a positive voltage is applied to the gate terminal w.r.t source terminals, which induces a channel by drawing the electrons in the p-type substrate to accumulate near the surface of the SiO_2 layer.
- As the value of $\mathbf{V_{GS}}$ is increased by making gate terminal more positive, more and more the electrons accumulate leading to an enhanced flow of drain current. Hence these MOSFET's are called as Enhancement MOSFET.
- The level of gate-to-source voltage $\mathbf{[V_{GS}]}$ that leads to significant flow of drain current is referred to as threshold voltage and is denoted by $\mathbf{V_T}$.
- For fixed $\mathbf{V_{GS}}$, if we increase the $\mathbf{V_{DS}}$, $\mathbf{I_D}$ initially increases and gets saturated.
- Reduction in the channel width near the drain region. This effect is known as pinch-off effect.
- The value of drain-source voltage at which the drain current saturates is given by $\mathbf{V_{DS\ (sat)}}$.
- From the output characteristics curve, we can observe that the $\mathbf{V_{DS(sat)}}$ voltage increases with the increases in the applied gate-to-source voltage.
- Relationship between the $\mathbf{V_{DS(sat)}}$ and $\mathbf{V_{GS}}$ is given by equation $\mathbf{V_{DS(sat)} = V_{GS} - V_T}$
- Drain current is zero for the $\mathbf{V_{GS} < V_T}$. For $\mathbf{V_{GS} > V_T}$, the drain current is given by

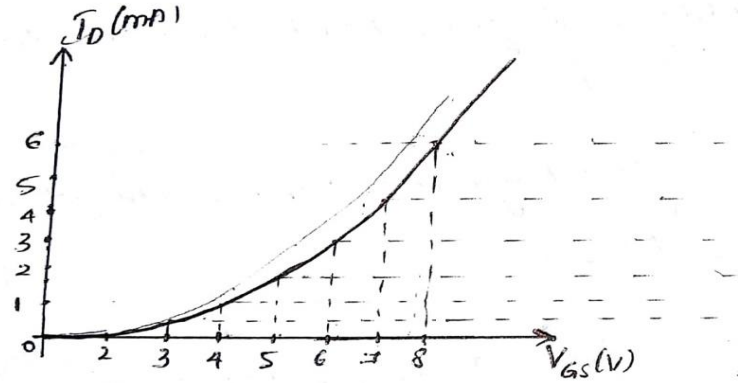
$$\mathbf{I_D = k[V_{GS} - V_T]^2}$$



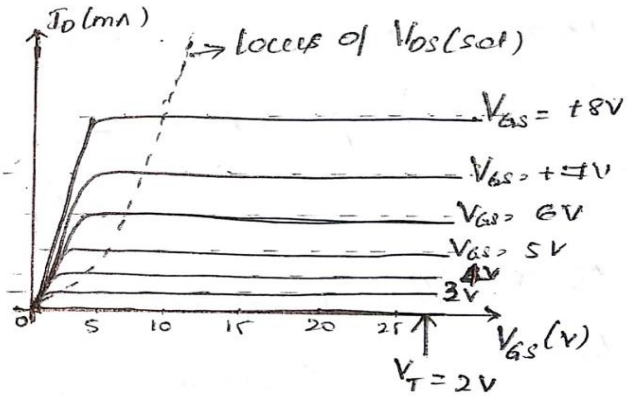




Pinch-off Phenomenon of E-MOSFET



Transfer Characteristics

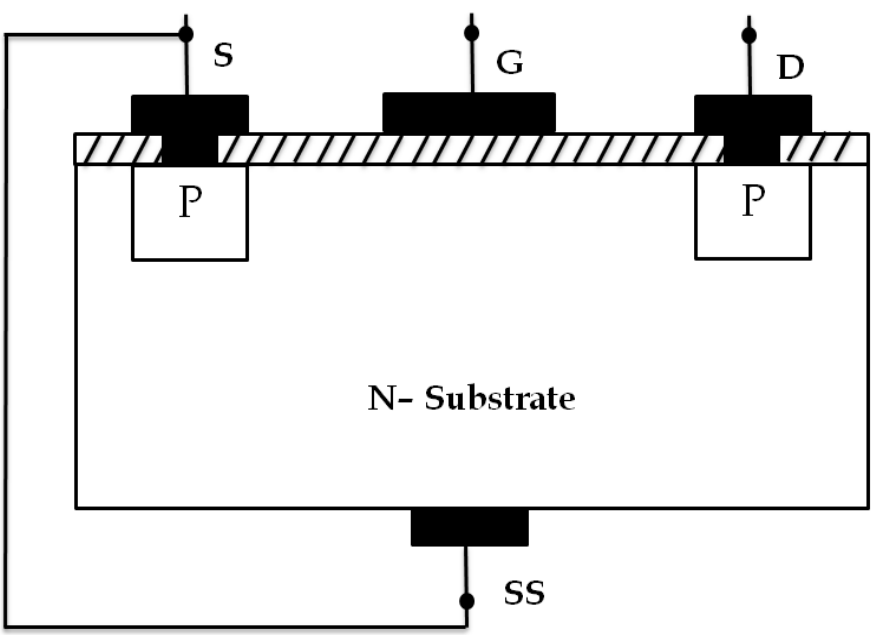


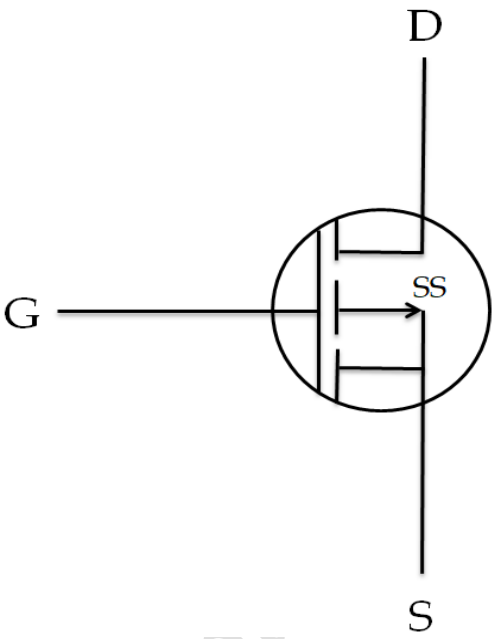
O/P Characteristics

P-channel Enhancement Type MOSFET:

Construction:

- Consider a slab of N-type substrate which is attached with a metallic contact called as Substrate terminal(SS).
- Two P-type materials are doped in the N-type substrate which is connected through the metallic contacts, which forms the two terminals namely Source(S) and Drain(D).
- Here there is no physical cannel between the source and the drain terminals.
- The P-channel E-MOSFET is as shown in the figure below and Dotted lines in the symbolic representation individuals the absence of channel.





Opeartion:

- When the gate-to-source voltage $\mathbf{V_{GS}}$ is zero and a voltage is applied between the drain and the source $\mathbf{V_{DS}}$ in the absence of n-channel will result in a current of effectively 0A.
- Drain current flows only when a negative voltage is applied to the gate terminal w.r.t source terminals, which induces a channel by drawing the electrons in the N-type substrate to accumulate near the surface of the SiO_2 layer.
- As the value of $\mathbf{V_{GS}}$ is increased by making gate terminal more negative, more and more the holes accumulate leading to an enhanced flow of drain current which is **reverse** to the **n-channel** DE MOSFET. Hence these MOSFET's are called as Enhancement MOSFET.
- The level of gate-to-source voltage [V_{GS}] that leads to significant flow of drain current is referred to as threshold voltage and is denoted by V_T.
- For fixed $\mathbf{V_{GS}}$, if we increase the $\mathbf{V_{DS}}$, $\mathbf{I_D}$ initially increases and gets saturated.
- Reduction in the channel width near the drain region. This effect is known as pinch-off effect.
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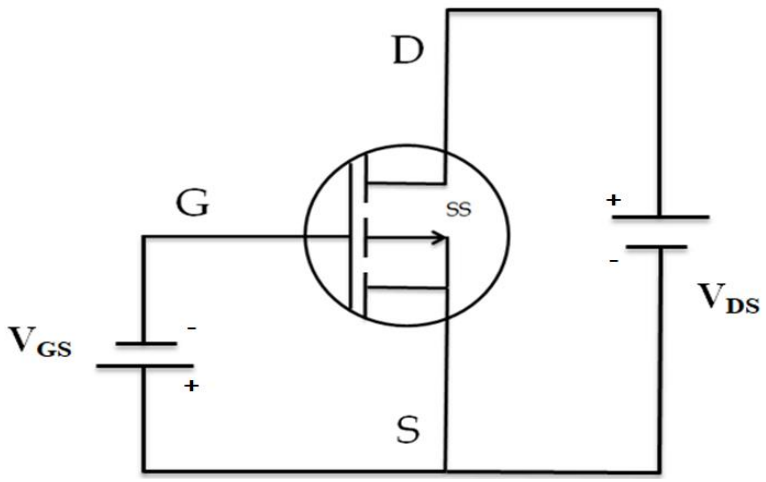
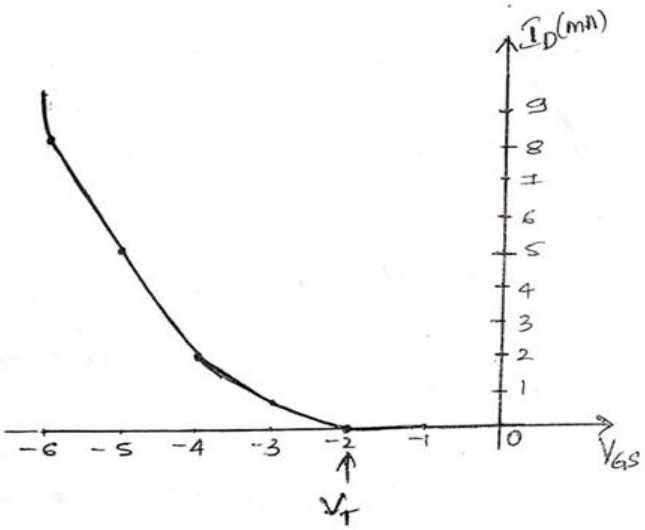
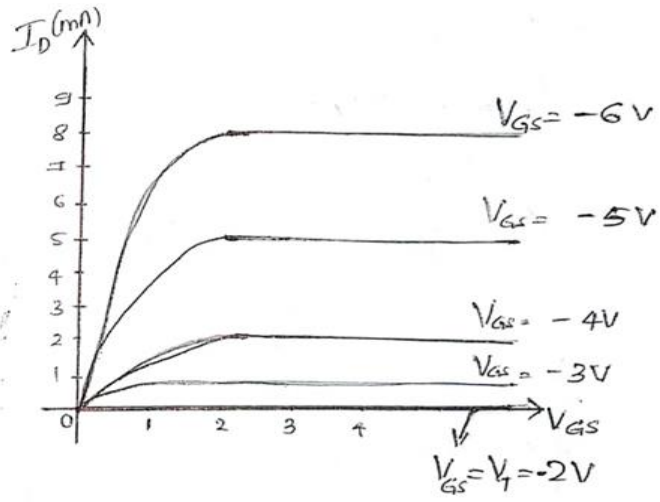
- From the output characteristics curve, we can observe that the $\mathbf{V_{DS(sat)}}$ voltage increases with the increases in the applied gate-to-source voltage $\mathbf{(V_{GS})}$.
- Relationship between the $\mathbf{V_{DS(sat)}}$ and $\mathbf{V_{GS}}$ is given by equation $\mathbf{V_{DS(sat)} = V_{GS} - V_T}$





TRANSFER CHARACTERISTIC CURVE

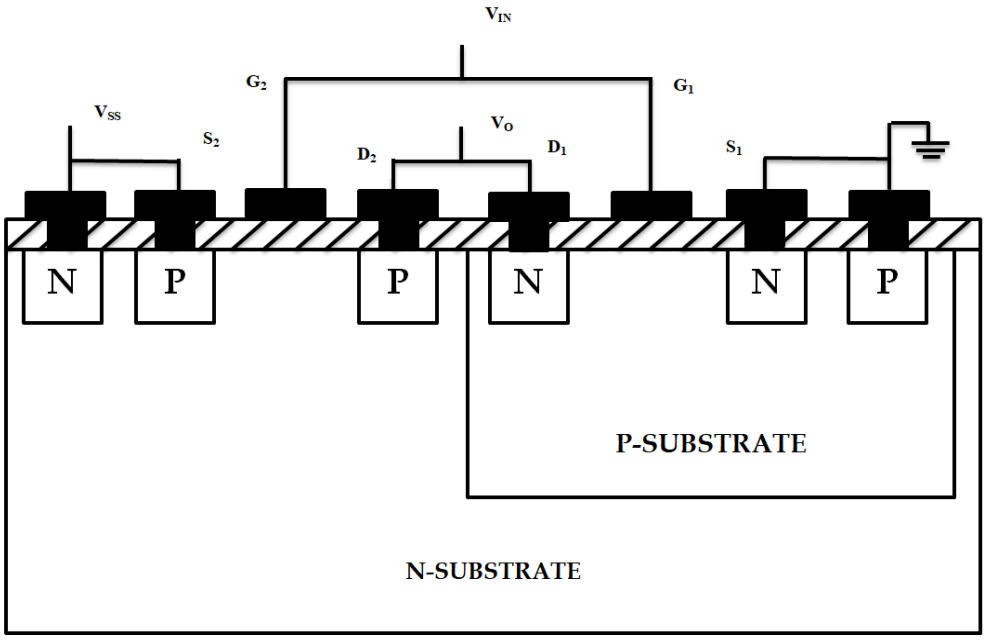


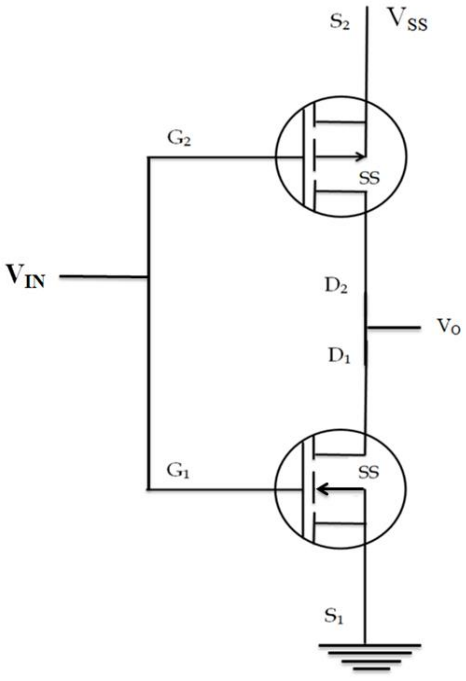
OUTPUT CHARACTERISTIC CURVE

CMOS:

Construction:

- Complementary Metal Oxide Semiconductor [CMOS] are those semiconductor device in which both P-channel and the N-channel E-MOSFET are diffused onto the same chip.
- CMOS configuration has extensive application in computer logic designs.
- CMOS devices offers high input impedance, low power consumption and require for less space as compared to BJT based logic circuit.
- CMOS offers slow switching speed compared to BJT's.
- Basic inverter circuit using CMOS configuration is as shown below.





- Inverter is a logic circuit that inverts the applied input signal, i.e. logic low input to logic high output and logic high input to logic low output.
- Complementary N-channel and P-channel E-MOSFET's are connected in series with gate terminals connected together to form the input terminal.
- Drain terminals are connected to form the output terminal.
- Source terminal of the P-channel MOSFET[S_2] is connected supply voltage V_{SS} and the source terminal of N-channel E-MOSFET[S_1] is connected to ground.

Operation:

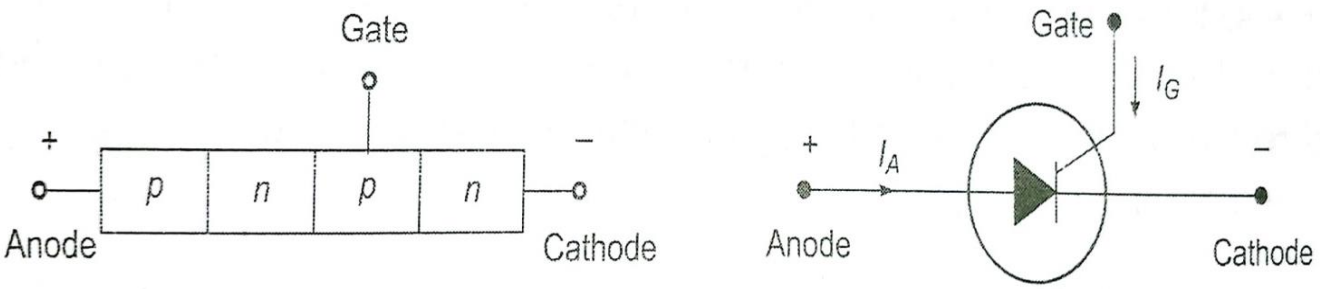
- When the input voltage $\mathbf{V_{IN}}$ is at logic low, the gate source voltage $\mathbf{[V_{G2S2}]}$ of the P-channel is equal to $\mathbf{-V_{SS}}$ and the MOSFET will be in the ON state, providing a low resistance path between $\mathbf{V_{SS}}$ and the output terminal.
- The gate-source voltage of N-channel is 0V [$\mathbf{V_{G1S1}}$] and therefore it is in the OFF state, resulting high impedance between the Output terminal [D_1] and ground [S_1].
- *Therefore output voltage $\boldsymbol{V_{out}}$ is equal to supply voltage V_{SS}. [i.e. for logic low input (V_I=0V), the output voltage is at logic high ($\boldsymbol{V_O=V_{SS}}$)*
- When $\mathbf{V_{IN}}$ is at logic high, that is equal to supply voltage $\mathbf{V_{SS}}$, the gate to source voltage [$\mathbf{V_{G2S2}}$] of the P-channel E-MOSFET is 0V and therefore MOSFET is in OFF state.
- The gate-source voltage of N-channel is equal to supply voltage $\mathbf{V_{SS}}$ and hence it is in ON state, resulting low resistance path.
- Two MOSFET's form a voltage divider and output voltage is approaching equal to 0 V.
- *Hence logic high input results in logic low output.*

Silicon Controlled Rectifier [SCR]:

- It is a four-layer device which has wide range of applications like rectifiers, regulated power supplies, dc to ac conversion (inverter), relay control, time delay circuits.
- SCR; are used to control high power of 10MW with individual rating of 2KA and 1.8KV with frequency range extended upto 50 KHz.

Operation:

- The material used for SCR is silicon because of high-temperature requirement of handling large current and power.
- Its four layers is arranged as pnpn shown in figure (a) and the outer layers are connected to terminals to form Anode (positive terminal) and Cathode (negative terminal) and the p layer closer to the cathode terminal is connected to the Gate terminal.
- The SCR symbol is drawn in the figure (b).



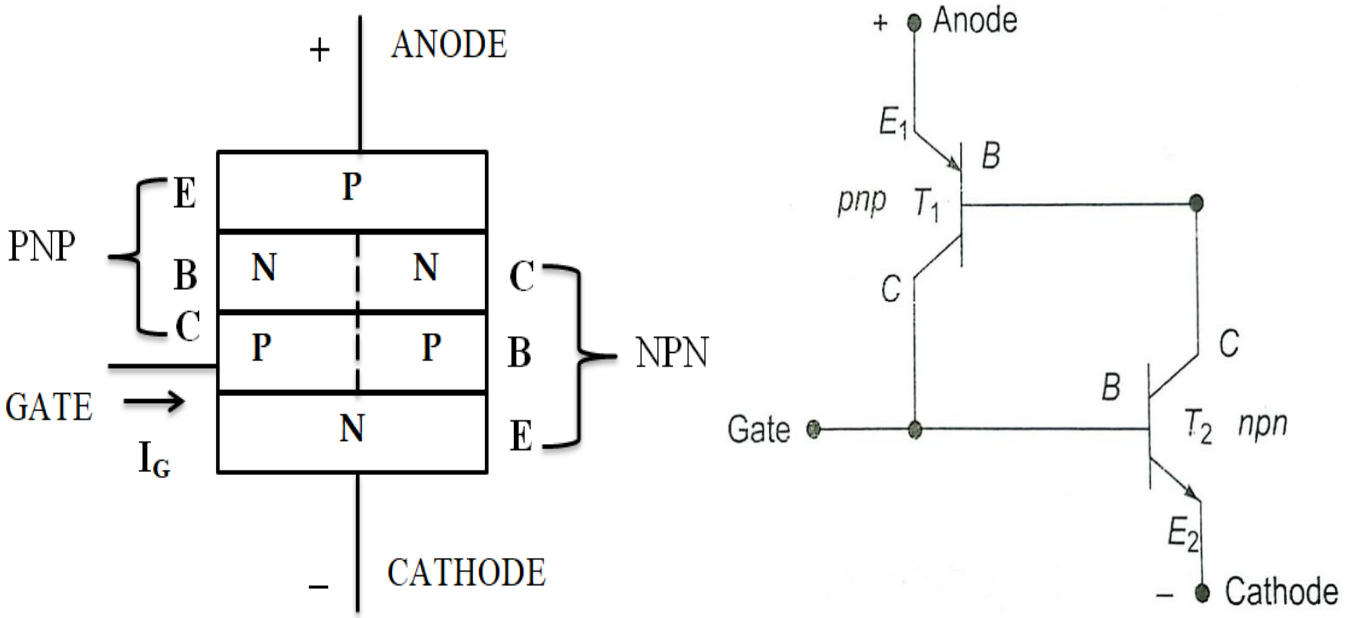
(a) Basic layout (b) Symbol

- As the forward voltage is applied across the anode and cathode, no conduction takes place as the middle ***np*** junction is reverse biased.

- If a positive pulse is applied at the gate terminal, such that a current of magnitude equal to or more than I_G (turn-on) flows into the gate, the processes in the device cause it to go into the conduction.
- The forward current is offered a resistance as low as 0.01 Ω to 0.1Ω.
- Because of regenerative action, removing the gate current does not cause the device to turn off.
- The dynamic resistance of SCR is as high as 100 K Ω or more.

Two Transistor Model:

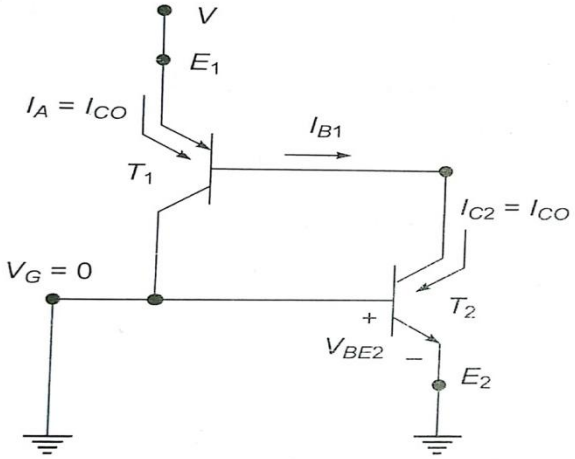
- The cross-sectional view of an SCR with the four layers is drawn as shown below in figure (a).
- The middle n and p layers can be imagined to be subdivided into two halves, as shown by the dotted line.
- Now it can be recognised that the device comprises one ***PNP*** and one ***NPN*** transistor.
- Since there is connectivity between two halves of each of these layers, the **Base** of the ***PNP*** is connected to the **Collector** of ***NPN*** and the **Collector** of ***PNP*** is connected to the **Base** of the ***NPN***, while the ***Gate*** is connected to the **Base** of ***NPN***.
- The corresponding two transistor model equivalent circuit is as shown below in the figure (b).



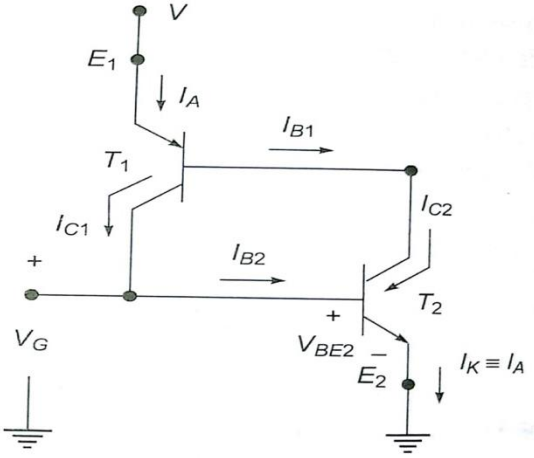
Switching Action:

- Let a positive voltage V be applied to the anode (E_1) and the cathode (E_2) and gate (G) be both grounded as shown in figure (a).
- As $\mathbf{V_G = V_{BE2} = 0}$, the transistor $\mathbf{T_2}$ is in 'OFF' state.
- It means that CB-junction of $\mathbf{T_2}$, through EB-junction of $\mathbf{T_1}$, is reverse biased.
- Therefore, $\mathbf{I_{B1} = I_{CO}}$ (minority carrier current) is too small to 'turn-on' $\mathbf{T_1}$.
- Thus both $\mathbf{T_1}$ and $\mathbf{T_2}$ are 'OFF' and so anode current $\boldsymbol{I_A = I_{B1} = I_{CO}}$ is of negligible order.
- It means that SCR is in 'turn-off' state, that is the switch between anode (E_1) and cathode (E_2) is open.
- Now, let a voltage $+V_G$ be applied at the gate as shown in figure (b), as $\mathbf{V_{BE2} = V_G}$, on making $\mathbf{V_G}$ sufficiently large, $\mathbf{I_{B2}}$ will cause T_2 to turn on and the collector current I_{C2} becomes large.
- As $\mathbf{I_{B1} = I_{C2}}$, T_2 turns on causing a large collector current $\mathbf{I_{C1}}$ **(I_A=I_{C1})** to flow.
- This in turn, increase I_{B2} causing a regenerative action to set in.

- The result is that the SCR is turned on, that is, the switch between the anode (E_1) and cathode (E_2) is closed (turn-on).
- The current $\mathbf{I_A}$ must be limited by the external circuit, say a series resistance between the source and E_1.
- The turn on time of an SCR is typically **0.1 to 1μs**.



(a) With $V_G = 0$



(b) With voltage V_G applied

Turn-Off:

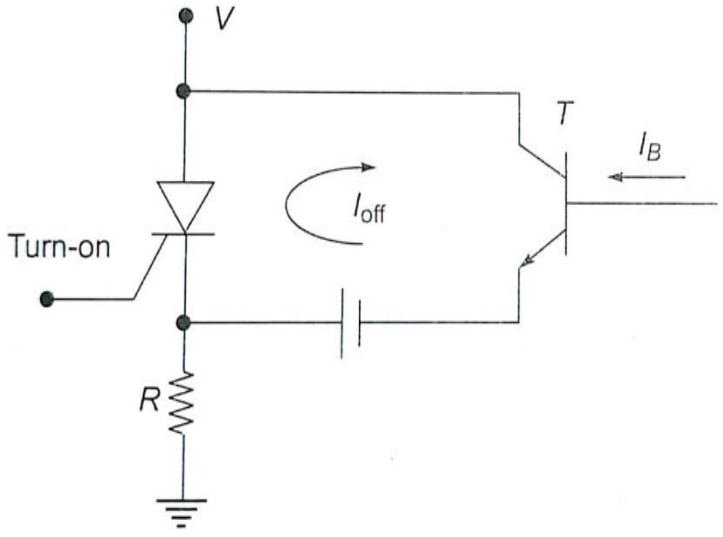
When the SCR is in conduction mode, the gate is ineffective in turning it off. The turn-off mechanism is called Commutation and it can be achieved in two ways explained below.

Natural Commutation:

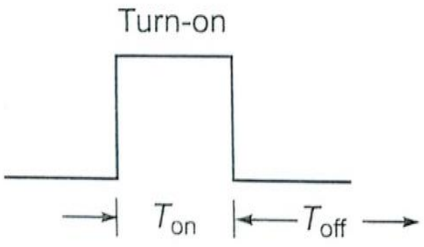
When the source that feeds the current to anode of SCR is such that it naturally passes through zero, the SCR turns off at the current zero. This is the case when the SCR is fed from the AC sources. In this situation, the commutation is also known as *line commutation*.

Forced Commutation:

In this method of commutation, the current through the SCR is forced to become zero by passing a current through it in opposite direction from an independent circuit.



(a) Circuit

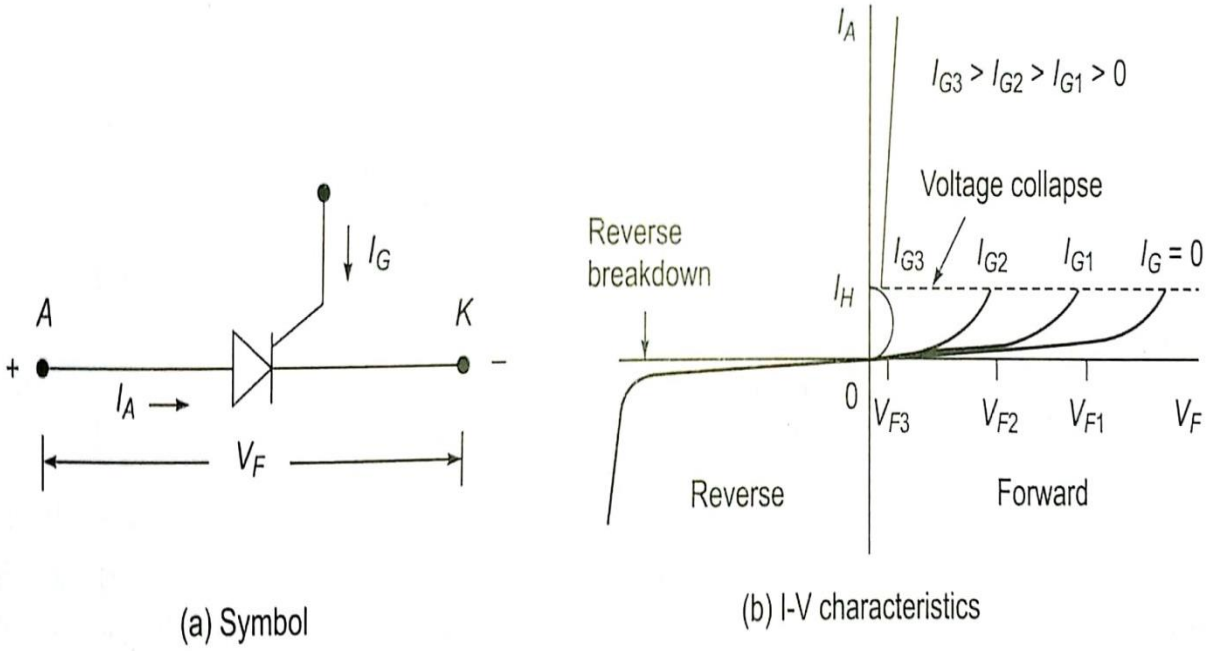


(b) Output waveform

SCR Characteristics:

The symbol and I-V characteristics of SCR are given below. Various voltages and current ratings of SCR are described below:

1. ***Forward Breakover Voltage V_F (BR):*** It I is the voltage at which for a given I_G, the SCR enters into conduction mode. From the below graph we can see that, this voltage reduces as I_G increases. V_F (BR) has dependence on the circuit connection between G and K terminals.
2. ***Holding Current I_H:*** It is the value of the current below which SCR switches from conduction state to forward blocking region of specified conditions.
3. Forward and Reverse blocking regions are those regions in which the SCR is open circuited and no current flows from anode to cathode.
4. Reverse breakdown voltage corresponds to Zener or Avalanche region of a diode.

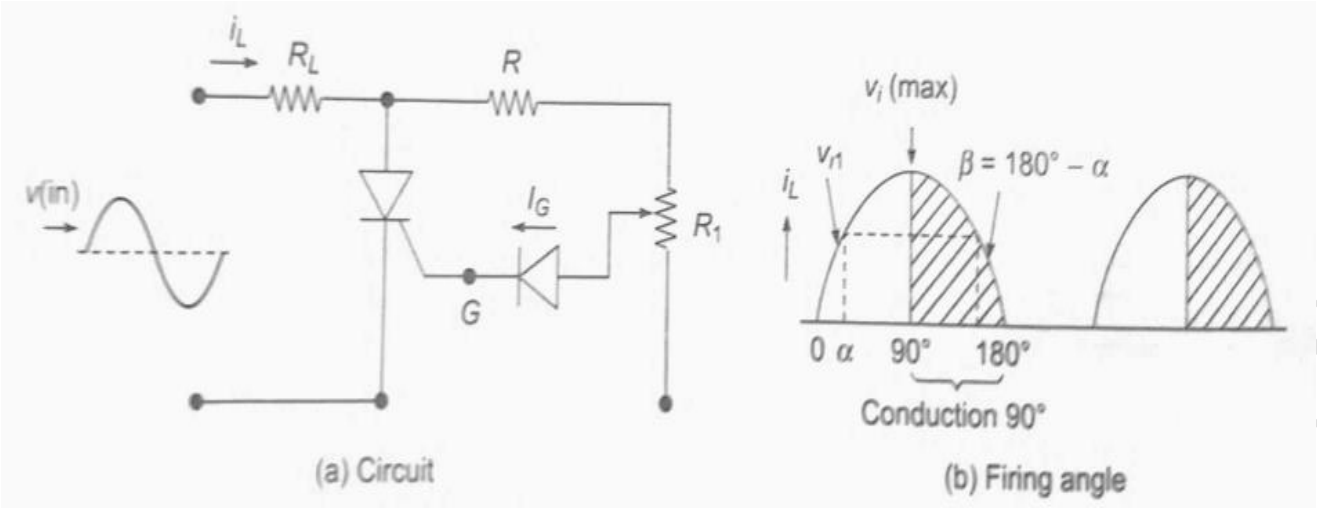


(a) Symbol

(b) I-V characteristics

SCR Application:

- One of the applications of SCR we are studying is, Variable Resistance Phase controlled.
- A variable-resistance phase control circuit is as shown below in figure (a).
- The SCR gate current is controlled through the resistance R and the variable resistance R_1.
- Let the RG be adjusted to high value so that even at the peak value v_i positive, $\mathbf{I_G < I_{G(turn\ on)}}$ and no conduction takes place.
- As $\mathbf{R_1}$ is reduced, $\mathbf{I_G}$ rises to turn-on value at the particular angle (time) of v_i.
- The conduction then begins and continues till $\mathbf{V_I}$ reaches zero(180^o).
- Varying $\mathbf{R_1}$ allows adjusting the SCR firing angle from 0^0 to 90^0 as shown in the figure (b) below.
- At $\mathbf{R_1}$, corresponding to the firing angle of $\mathbf{90^0}$, $\mathbf{V_I=V_{I(max)}}$. If R1 is adjusted for firing at α, the firing will take place at angle $\boldsymbol{\alpha < 90^0}$ but not at angle but not at angle $\boldsymbol{\beta = (180^0 - \alpha) > 90^0}$ as the angle α is reached earlier in time on the $\mathbf{V_I}$ wave.
- So the operation of this circuit is known as *half-wave*, *variable-resistance phase control*.

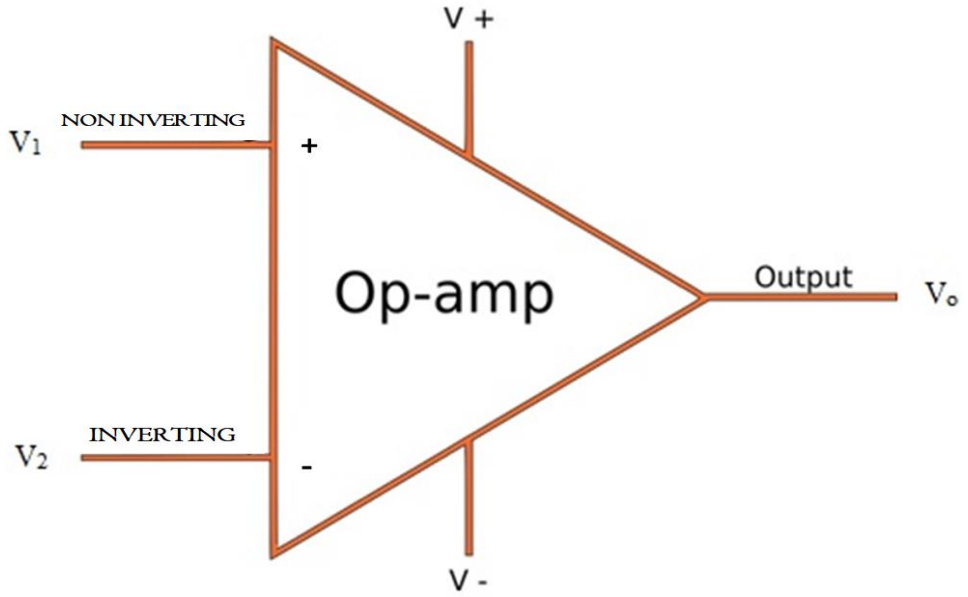


- Thus $\mathbf{I_{L(DC)}}$ can be adjusted to the maximum value at 0^0 to the minimum value at 90^0.

MODULE 3

OPERATIONAL AMPLIFIERS & APPLICATIONS

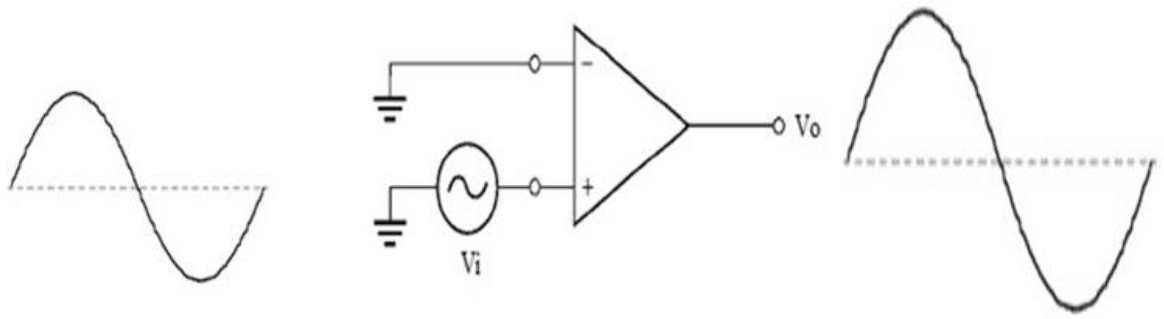
- An operational amplifier or Op-Amp is a ***high gain differential amplifier*** with ***high input impedance*** and ***low output impedance***.
- Operational amplifiers are used to ***provide voltage amplitude changes***, ***Oscillators***, ***filter circuit*** etc.
- An op-amp contains ***different amplifier stages*** to achieve a ***very high voltage gain***.
- An op-amp consists of two input terminals ***(Inverting and Non Inverting)*** and one output terminal which works as differential amplifier. It is as shown in the figure below.



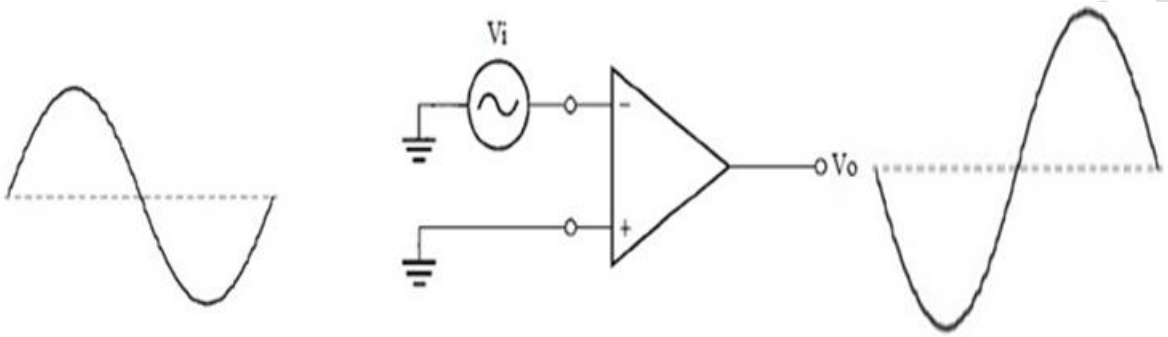
- Each input results in either the same or an opposite polarity output depending on whether the input signal is applied to the Non-inverting terminal or inverting terminal.
- Based on the input modes, op-amps are classified as:
  - **Single Ended Input**
  - **Double Ended Input *[Differential Mode]***
  - **Common Mode Operation**

1. ***Single Ended Mode:***

- Single ended input operation results when the input signal is connected to one input with the other input terminal connected to ground.
- Figure (a) shows the input is applied to Non-inverting terminal, connecting inverting terminal to ground, which results in an output having the same polarity as the input signal.
- Figure (b) shows the input is applied to Inverting terminal, connecting Non-inverting terminal to ground, which results in an output which is opposite in phase to the applied input signal.



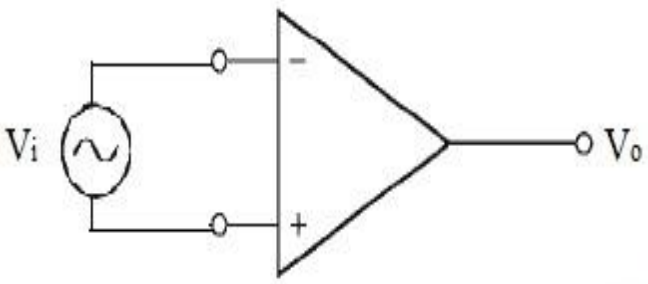
(a) Non-inverting amplifier



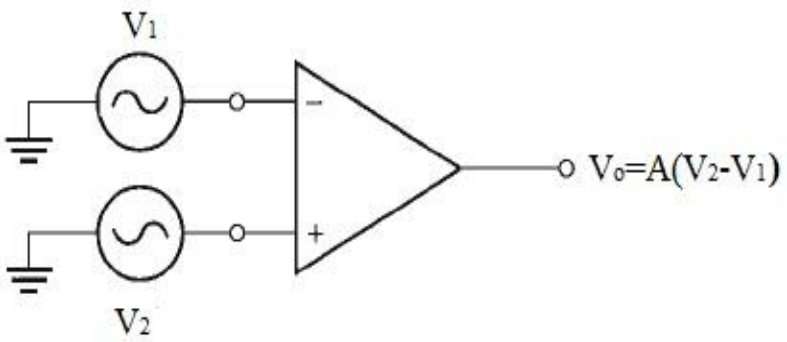
(b) Inverting amplifier

2. ***Double Ended Mode or differential Mode:***

- When the input is applied to both the input terminals it is called double ended operation of differential mode operation.
- Figure below shows an input V_i is applied between the two input terminals with the resulting amplified output in phase with the applied input between the non-inverting and inverting terminal.

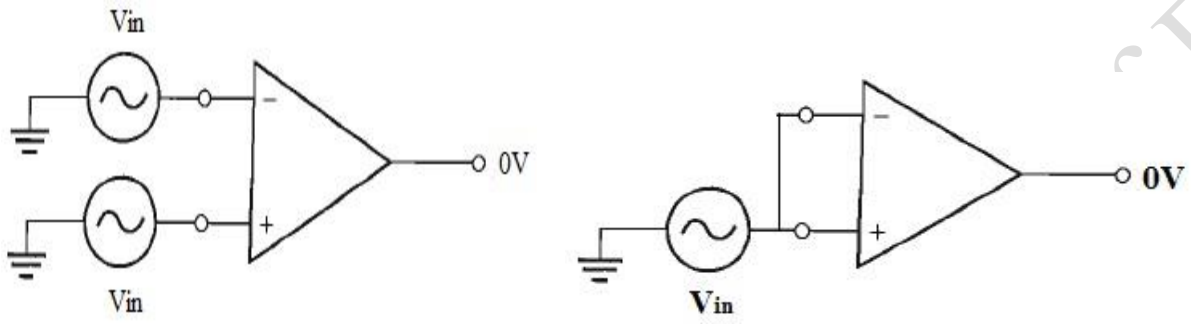


- Figure below shows two inputs V1 and V2 are applied to inverting and non-inverting terminals of an Op-amp which produces the output which is the difference signal (V2-V1) being amplified.



3. ***Common Mode operation or common Mode Rejection***

- In common mode, two signals voltages of the same phase, frequency and amplitude are applied to the two inputs as shown in fig below.
- When equal input signals are applied to both inputs, they cancel, resulting in a zero output voltage. This action is called common-mode rejection.
- But practically, a small output signal will result.
- The overall operation amplifies the difference signal while rejecting the common signal at the two inputs.



Op-amp parameters

1. ***Common Mode Rejection Ratio (CMRR):***

- The measure of an amplifiers ability to reject common-mode signal is called Common-Mode Rejection.
- It can also be defined as the ratio of Differential gain (A_d) to the Common mode gain (A_c)

$$\mathbf{CMRR = \frac{A_d}{A_c}}$$

- CMRR is often expressed in decibels (dB) as

$$\mathbf{CMRR = 20 \log \left(\frac{A_d}{A_c}\right) dB}$$

- Higher the CMRR better is the performance of Op-amp.

2. ***Input Offset Voltage and Input Offset Current:***

- The ideal Op-amp produces zero volts output for zero volts input.
- In a practical Op-amp, a small DC voltage appears at the output when no differential voltage is applied.
- The difference between the voltages present between the two input terminals when zero voltage is applied is called as ***"Input offset Voltage, V_{OS}"***.

$$\mathbf{V_{OS} = I_{OS} R_{in}}$$

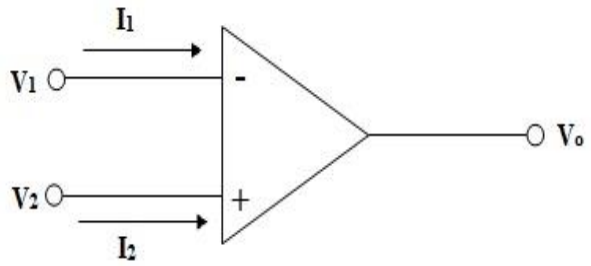
- In ideal op-amp, the two input bias currents are equal and thus their difference is zero.
- In a practical Op-amp the bias current is not exactly zero.
- The difference of the input bias currents is called as ***"Input offset current, I_{OS}"***, expressed as an absolute value.

$$\mathbf{I_{OS} = |I_1 - I_2|}$$

3. Input bias current:

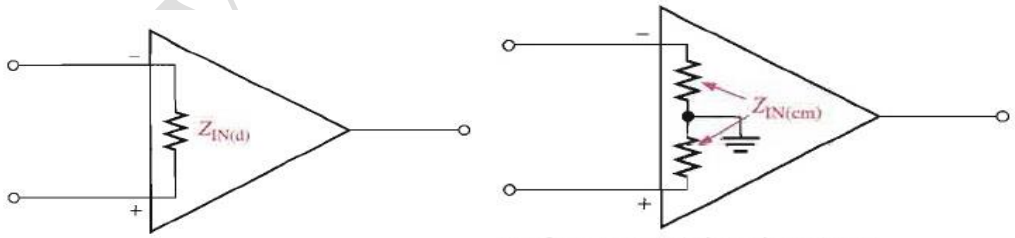
- The input bias current is the DC current required by the inputs of the amplifier to properly operate the first stage.
- The input bias current is the average of both input currents and can be calculated as follows:

$$I_{Bias} = \frac{I_1 + I_2}{2}$$



4. Input Impedance:

- Two basic ways of specifying the input impedance of an Op-amp are the differential mode and common mode.
- The ***Differential Input Impedance*** is the total resistance between the inverting and the non-inverting inputs as shown in figure (a).
- Differential impedance is measured by determining the change in bias current for a given change in different input voltage.
- The ***Common Mode Input Impedance*** is the resistance between each input and ground as shown in figure (b).
- It is measured by determined the change in bias current for a given change in common-mode input voltage.



(a) Differential input impedance (b) Common-mode input impedance

5. Output impedance:

- Output impedance is the resistance viewed from the output terminal of the Op-amp, as shown in figure below.

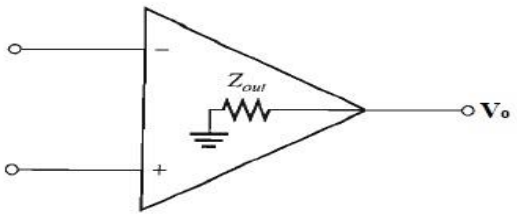
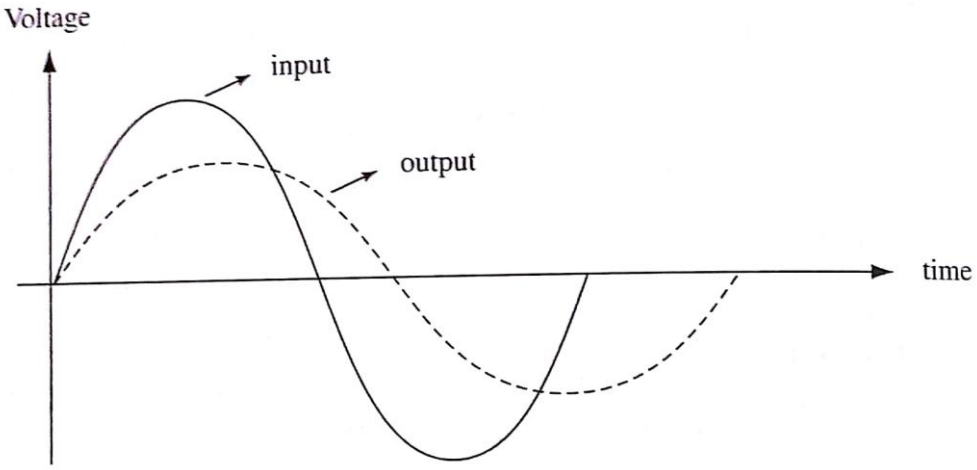


Fig 7: Op-amp Output impedance

6. Slew rate:

- Slew rate (SR) or Maximum Slew rate (MSR) is defined as the maximum rate of change of output voltage with respect to time.
- Slew rate can be expressed in Volts per microsecond.

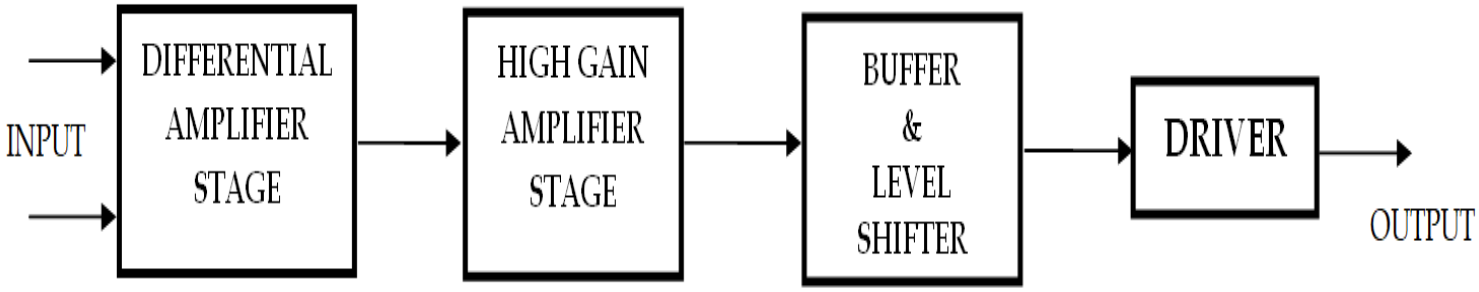
$$\textbf{SR or MSR} = \frac{\Delta \mathbf{V_{out}}}{\Delta \mathbf{t}}\ \mathbf{V/\mu s}$$



Characteristics of an ideal Op-amp:

- ***Infinite voltage gain (A= ∞):*** The voltage gain of an ideal Op-amp is infinite.
- ***Infinite input impedance ($R_i = Z_i = \infty$):*** An ideal Op-amp does not draw any current from the voltage sources connected to its input terminal.
- ***Zero output impedance ($R_o = 0$):*** The output voltage of an ideal Op-amp is independent of the current drawn from it.
- ***Infinite Bandwidth (BW= ∞):*** An ideal Op-amp amplifies signals of any frequency with a constant gain.
- ***Infinite CMRR (CMRR (ρ)= ∞):*** The common-mode rejection ratio of an ideal Op-amp is infinite.
- ***Infinite Slew rate (SR= ∞):*** The output voltage changes simultaneously with the input voltage.
- ***Power Supply Rejection Ratio (PSRR=0)***: The power supply rejection ratio is zero.
- ***Zero offset voltage***: The presence of small output voltage when $V_1=V_2=0$ is called an offset voltage.
- The characteristics of an ideal Op-amp do not change with temperature.

Block diagram of an Op-amp:



- The symbol and Block diagram of an op-amp is as shown above.
- It has different blocks namely, Differential amplifier, High Gain Amplifier, Buffer and Level shifter and the Driver.

1. Differential Amplifier:

- It is the input stage of the Op-amp.
- It amplifies the difference of inputs i.e., (V_1-V_2)

2. High gain Amplifier:

- The output of differential amplifier stage is given as input to the High Gain Amplifier stage.
- This stage provides very high gain through a direct coupled amplifier.

3. Buffer and Level Shifter:

- The buffer is an emitter follower for matching the load.
- If the output is non-zero input, the level shifter makes it zero.

4. Driver:

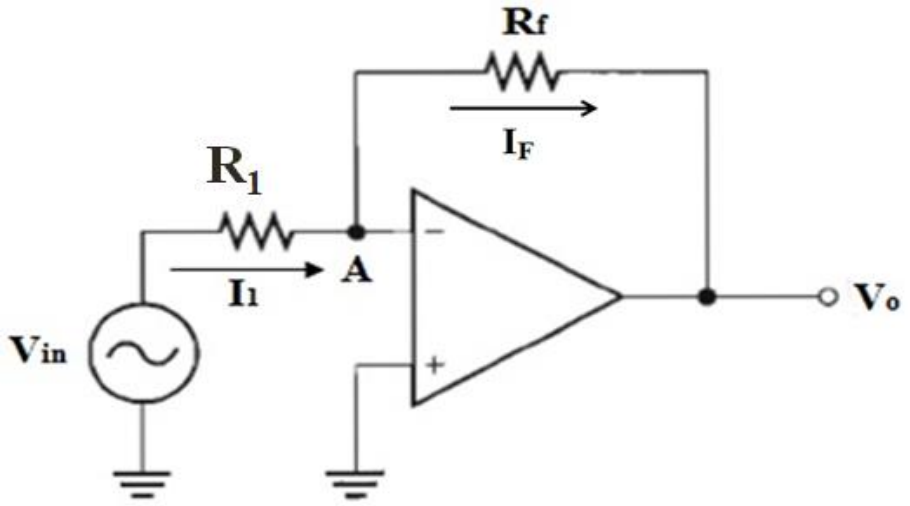
- It is a power amplifier used at the output stage.
- It produces very high amplified signals with respect to the input.

Applications of Op-amp

i. ***Inverting amplifier***
ii. ***Non-inverting amplifier***
iii. ***Adder or Summing Amplifier***
iv. ***Voltage follower***
v. ***Integrator***
vi. ***Differentiator***
vii. ***Comparator***

i) Inverting amplifier

- The Inverting amplifier circuit is as shown in figure below.



- The input is applied to the inverting terminal of the Op-amp and Non-inverting terminal is grounded.
- The potential at V_A will be zero because of virtual ground concept which states that both the input terminal will be at same potential. [**$V_A = V_B$ (VIRTUAL GROUND)**]
- Also current to the input terminal of Op-amp is zero as $R_{in}=\infty$.
- Applying KCL at node A, $\mathbf{I_1 = I_F}$

$$\mathbf{I_F = I_1}$$

$$\frac{V_A - V_o}{R_F} = \frac{V_{in} - V_A}{R_1}$$

$$\frac{0 - V_o}{R_F} = \frac{V_{in}}{R_1}$$

$$\frac{-V_o}{R_F} = \frac{V_{in}}{R_1}$$

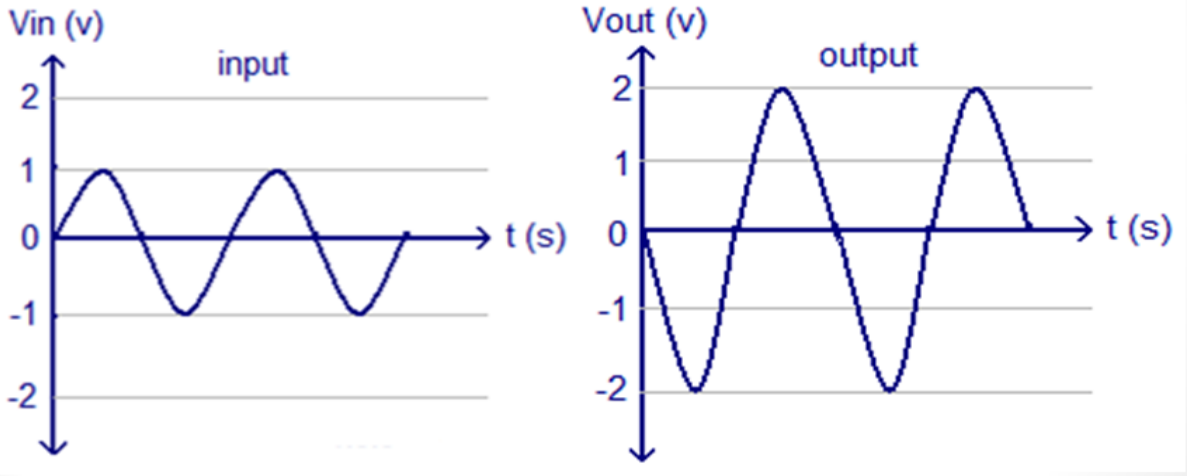
$$\frac{V_o}{V_{in}} = \frac{-R_F}{R_1}$$

$$\textbf{Amplifier Gain} \quad A = \frac{V_o}{V_{in}}$$

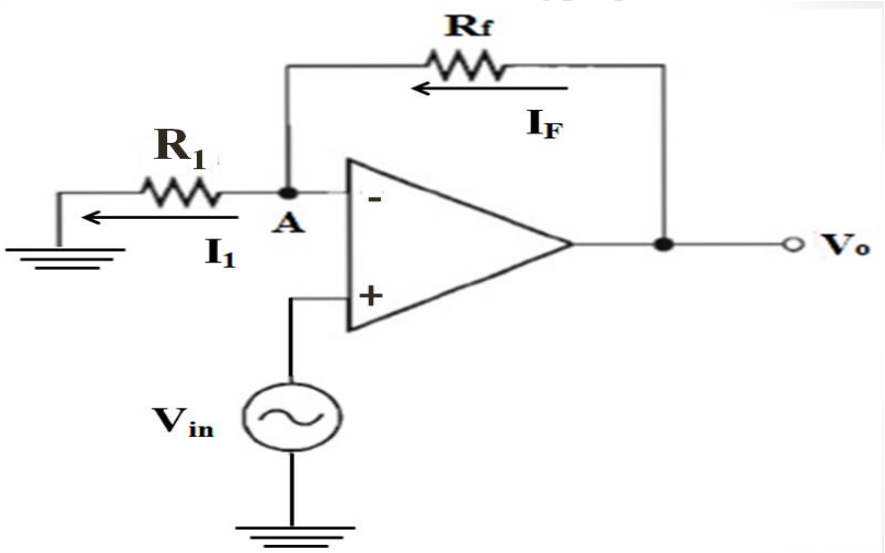
$$A = \frac{-R_F}{R_1}$$

$$V_o = A V_{in} \quad ; \quad V_o = -\left(\frac{R_F}{R_1}\right) V_{in}$$

- The output is the amplified output which is negative to the input i.e., Inverted.
- The negative sign indicates that the polarity of the output is opposite to that of input, as shown below.



ii) Non-Inverting Amplifier:



- The Non-Inverting amplifier circuit is as shown above.
- Input is applied to the Non-Inverting terminal of the Op-amp and Inverting terminal is grounded.
- The potential at node A is equal to V_{in} because of virtual ground concept, i.e., $\mathbf{V_A = V_{in}}$
- Applying KCL at node A,

$$\mathbf{I_F = I_1}$$

$$\frac{V_o - V_A}{R_f} = \frac{V_A - 0}{R_1}$$

$$\frac{V_o}{R_f} = \frac{V_{in}}{R_1} + \frac{V_{in}}{R_f}$$

$$\frac{V_o}{R_f} = V_{in}\left(\frac{1}{R_1} + \frac{1}{R_f}\right)$$

$$\frac{V_o}{V_{in}} = R_f\left(\frac{1}{R_1} + \frac{1}{R_f}\right)$$

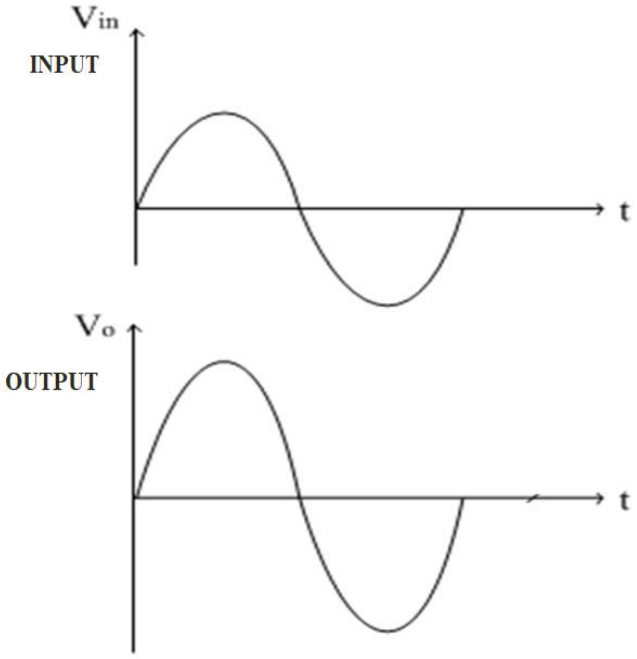
$$\frac{V_o}{V_{in}} = \left(\frac{R_f}{R_1} + \frac{R_f}{R_f}\right)$$

$$\frac{V_o}{V_{in}} = \left(\frac{R_f}{R_1} + 1\right), \qquad \frac{V_o}{V_{in}} = \left(1 + \frac{R_f}{R_1}\right)$$

$$A = \left(1 + \frac{R_f}{R_1}\right),$$

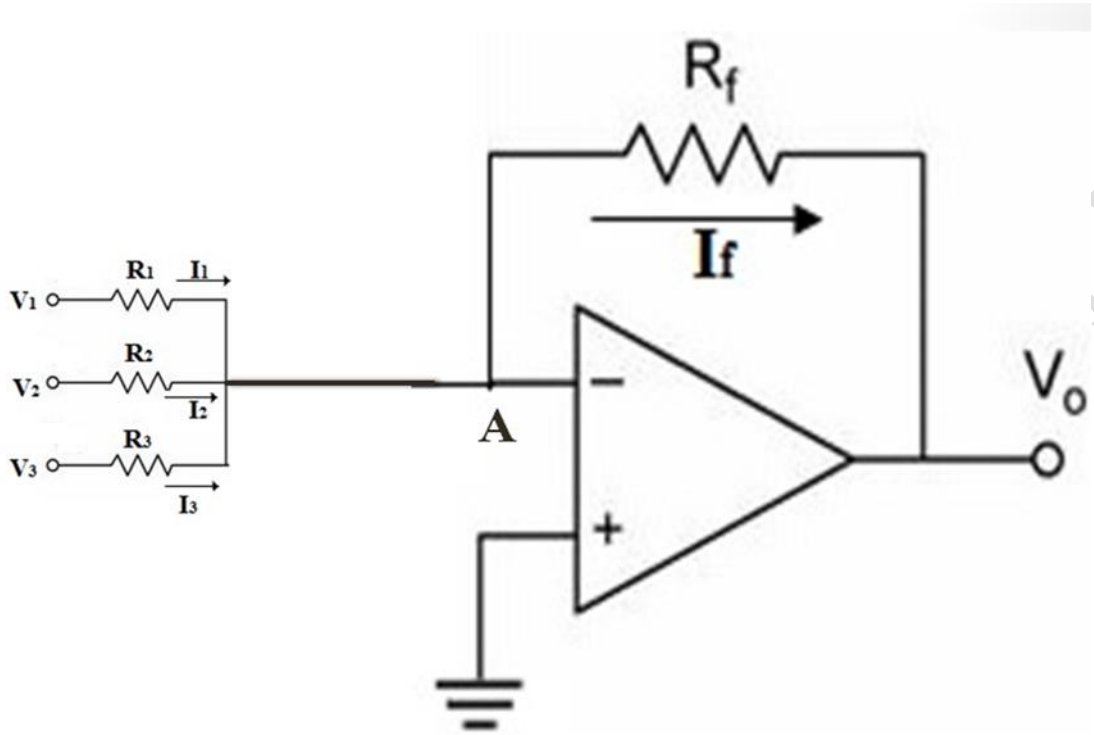
$$V_o = V_{in}\left(1 + \frac{R_f}{R_1}\right)$$

- Output has the same sign of input. Hence it is in phase. Therefore, it is Non-inverting.



iii) Summing Amplifier [Inverting]:

- When more than one input is applied to either the inverting or to the non-inverting terminal, the output will be sum of all the voltages applied, each multiplied by a constant gain.



- Consider the Op-amp circuit shown above which has 3 inputs V_1, V_2 and V_3 given to the inverting terminal, through R_1,R_2, &bR_3 respectively.
- Applying KCL to node A; $\mathbf{I_1+I_2+I_3 = I_F}$

$$\mathbf{I_F = I_1 + I_2 + I_3}$$

$$\mathbf{\frac{-V_o}{R_f} = \frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3}}$$

$$\mathbf{V_o = -\left\{R_f\left(\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3}\right)\right\}}$$

$$\mathbf{V_o = -\left\{\left(\frac{R_f}{R_1}\right)V_1 + \left(\frac{R_f}{R_2}\right)V_2 + \left(\frac{R_f}{R_3}\right)V_3\right\}}$$

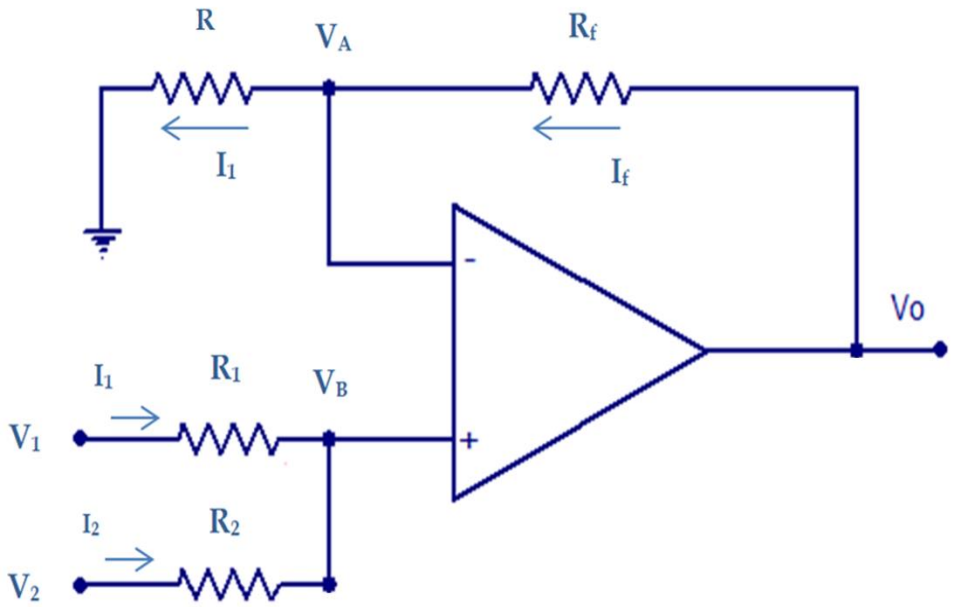
Each signal is amplified with Gain and then gets Added

If we assume $\mathbf{R_1 = R_2 = R_3 = R_f = R}$,

$$\mathbf{V_o = -(V_1 + V_2 + V_3)}$$

iv) Summing Amplifier [Non-Inverting]:

- When more than one input is applied to either the inverting or to the non-inverting terminal, the output will be sum of all the voltages applied, each multiplied by a constant gain.



- Consider the Op-amp circuit shown in the figure above which has 2 inputs V_1 and V_2 given to the inverting terminal.
- Voltage at the node A $\mathbf{V_A}$ is at the same potential of as of node B V_B. $\mathbf{V_A = V_B}$
- From the input side: $$\mathbf{I_1 + I_2 = 0}$$

$$\mathbf{But,\ I_1 = \frac{V_1 - V_B}{R_1}} \quad \text{and} \quad \mathbf{I_2 = \frac{V_2 - V_B}{R_2}}$$

$$\mathbf{I_1 + I_2 = 0}$$

$$\mathbf{\frac{V_1 - V_B}{R_1} + \frac{V_2 - V_B}{R_2} = 0}$$

$$\boldsymbol{V_B = \frac{R_2 V_1 + R_1 V_2}{R_1 + R_2}}$$

At node A

$$\mathbf{I_F = I_1}$$

$$\boldsymbol{\frac{V_o - V_B}{R_f} = \frac{V_A - 0}{R}}$$

$$\mathbf{V_A = V_B} \quad \textbf{(Due to Virtual ground)}$$

$$\frac{V_o - V_B}{R_f} = \frac{V_B}{R}$$

$$\frac{V_o}{R_f} = \frac{V_B}{R_f} + \frac{V_B}{R_1} = V_B\left(\frac{R+R_f}{R*R_f}\right)$$

$$V_O = V_B\left(\frac{R+R_f}{R}\right) = V_B\left(1 + \frac{R_f}{R}\right)$$

Substituting V_B value in the above equation, V_O becomes;

$$V_O = \left(\frac{R_2V_1+R_1V_2}{R_1+R_2}\right)\left(\frac{R+R_f}{R}\right) \quad = \left(\frac{R_2V_1+R_1V_2}{R_1+R_2}\right)\left(1 + \frac{R_f}{R}\right)$$

$$V_O = \left[\left(\frac{R_2\,(R+R_f)}{R\,(R_1+R_2)} * V_1\right) + \left(\frac{R_1\,(R+R_f)}{R\,(R_1+R_2)} * V_2\right)\right]$$

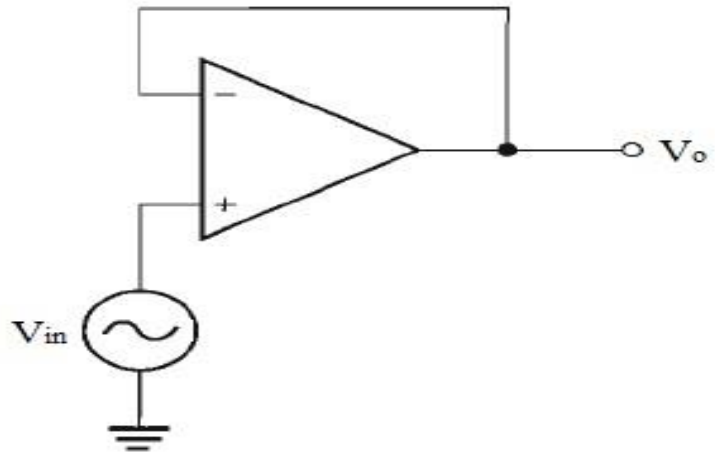
OR

$$V_O = \left[\left(\frac{R_2}{(R_1+R_2)} * \left(1 + \frac{R_f}{R}\right) * V_1\right) + \left(\frac{R_1}{(R_1+R_2)} * \left(1 + \frac{R_f}{R}\right) * V_2\right)\right]$$

Assuming $\mathbf{R_2 = R_1 = R_f = R}$

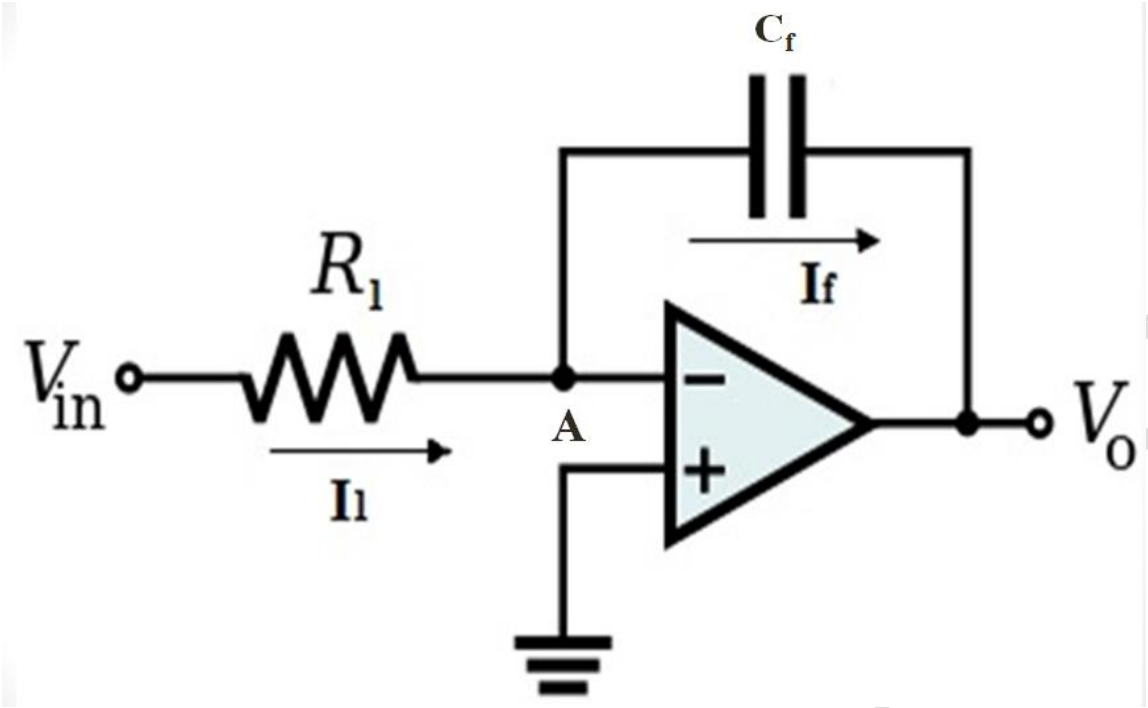
$$V_O = [V_1 + V_2] \qquad \text{(Sum of Two Inputs)}$$

v) Unity follower or Voltage follower:



- The voltage follower circuit is as shown above.
- It produces a unity gain with no polarity or phase reversal.
- The output will be equal to the input applied, i.e., $\mathbf{V_o = V_{in}}$
- This circuit is called as voltage follower because the output will be same as input.

vi) ***Integrator*:**



- If the feedback component used is a capacitor, the resulting connection is called Integrator and the circuit can be written as shown above.
- Considering the voltage at the junction of R and X_{Cf} to be ground (since $V_{in} \approx 0$), $\mathbf{I_F = I_1}$.
- Capacitive impedance can be expressed as:

$$\mathbf{I_1} = \frac{\boldsymbol{V_{in} - V_A}}{\boldsymbol{R_1}} \quad \& \quad \mathbf{I_F} = \frac{\boldsymbol{V_A - V_o}}{\boldsymbol{X_{Cf}}} = \mathbf{C_f}\frac{\boldsymbol{d(V_A - V_O)}}{\boldsymbol{dt}}$$

$\mathbf{V_A = V_B}$ **(**Due to virtual ground**);** $\mathbf{\therefore V_A = 0}$ $(\because V_B = 0)$

$$\mathbf{I_F = I_1}$$

$$-\mathbf{C_f}\frac{\boldsymbol{dV_O}}{\boldsymbol{dt}} = \frac{\boldsymbol{V_{in}}}{\boldsymbol{R_1}}$$

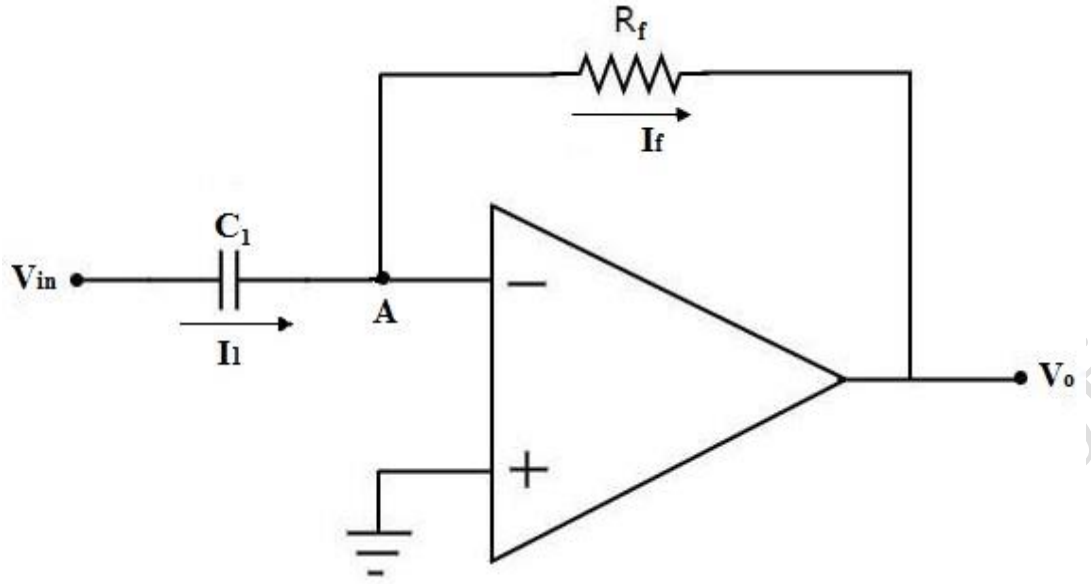
Integrating both side

$$\boldsymbol{V_o} = -\frac{\mathbf{1}}{\boldsymbol{R_1 C_f}}\int_{\mathbf{0}}^{\boldsymbol{t}} \boldsymbol{V_{in}}\, \boldsymbol{dt}$$

The above equation can be expressed in time domain as

$$\boldsymbol{V_o(t)} = -\frac{\mathbf{1}}{\boldsymbol{R_1 C_f}}\int_{\mathbf{0}}^{\boldsymbol{t}} \boldsymbol{V_{in}(t)dt}$$

vii) ***Differentiator:***



- In Differentiator circuit, the input is applied through capacitance C_1 as shown in the figure above.
- Considering the voltage at node A is zero because of virtual ground concept.

$$\mathbf{I_F = I_1}$$

$$\mathbf{I_f = \frac{V_A - V_O}{R_F}} \quad \& \quad \mathbf{I_1 = \frac{V_{in} - V_A}{X_c} = C_1 \frac{d(V_{in} - V_A)}{dt}}$$

$$\therefore \mathbf{V_A = 0} \qquad (\because V_B = 0)$$

$$\mathbf{-\frac{V_o}{R_F} = C_1 \frac{d(V_{in})}{dt}}$$

$$\mathbf{V_A = 0} \qquad (V_B = 0)$$

$$\boldsymbol{V_o = -R_F C_1 \frac{dV_{in}}{dt}}$$

viii) ***Comparator:***

- The Op-amp comparator circuit and the output are shown in figure (a) and (b).
- The saturation characteristic of an Op-amp in open loop is made use of in determining whether a signal is more or less than a certain reference value (V_R).
- If non-inverting terminal is grounded (V_R=0), the circuit becomes zero crossing detector.
- If V_i is sinusoidal, the output waveform will be rectangular assuming $\boldsymbol{\epsilon = 0}$.

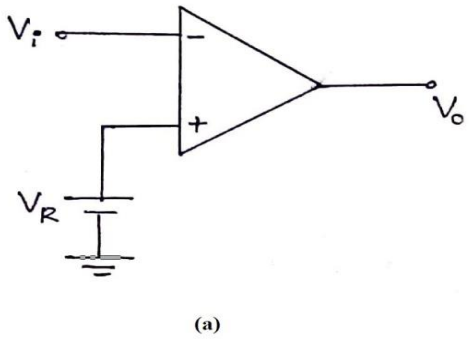


Fig (a): Op-amp Comparator circuit

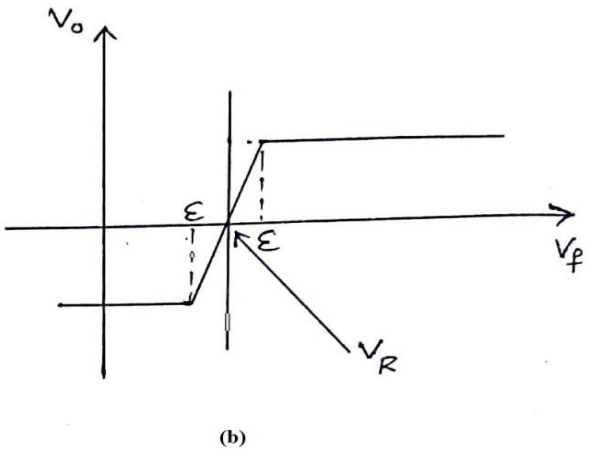


Fig (b): Comparator output

Transfer characteristics of Op-amp:

- An Op-amp is a linear device with high gain.
- For small value of $V_i = \epsilon$, the output will be very high, i.e., V_{CC}.
- Beyond that the output gets saturated.
- Circuit diagram for open loop Op-amp and transfer characteristic is as shown in figures (a) and (b).

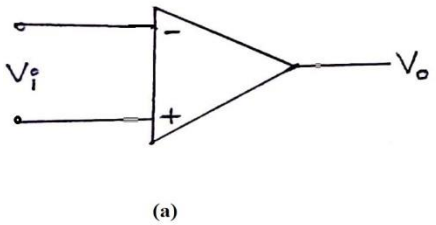


Fig (a): Open loop Op-amp

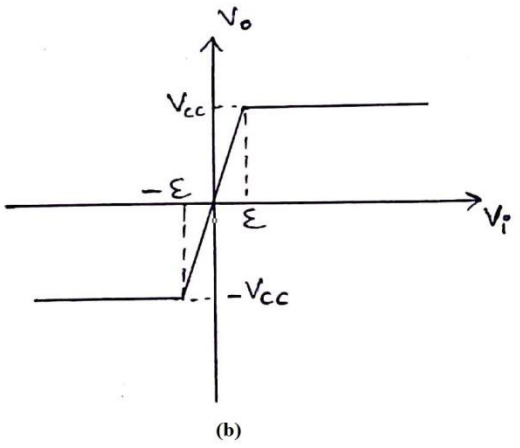


Fig (b): Transfer characteristics

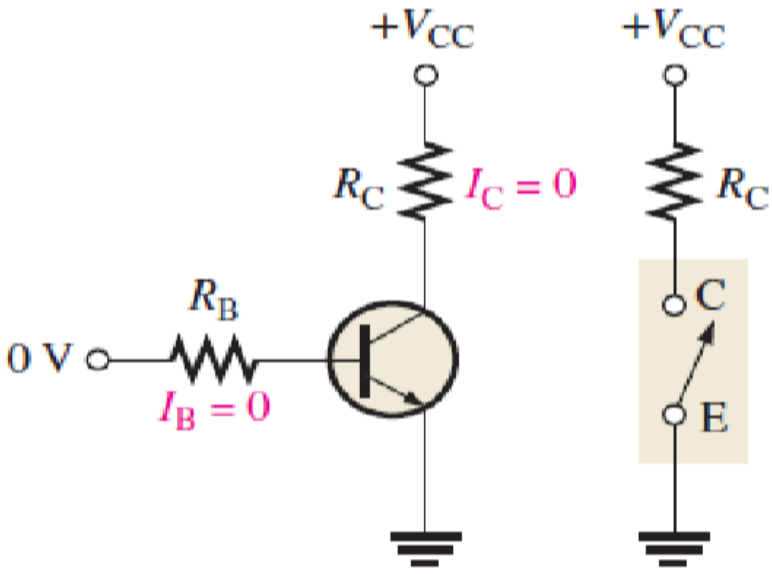
MODULE 4

BJT AMPLIFIER AND OSCILLATOR

Switching Operation [Transistor as a Switch]:

- Figure below illustrates the basic operation of a BJT as a switching device.
- The device will be **ON** in the *Saturation Region* and will be **OFF** in the *Cut-off Region*.

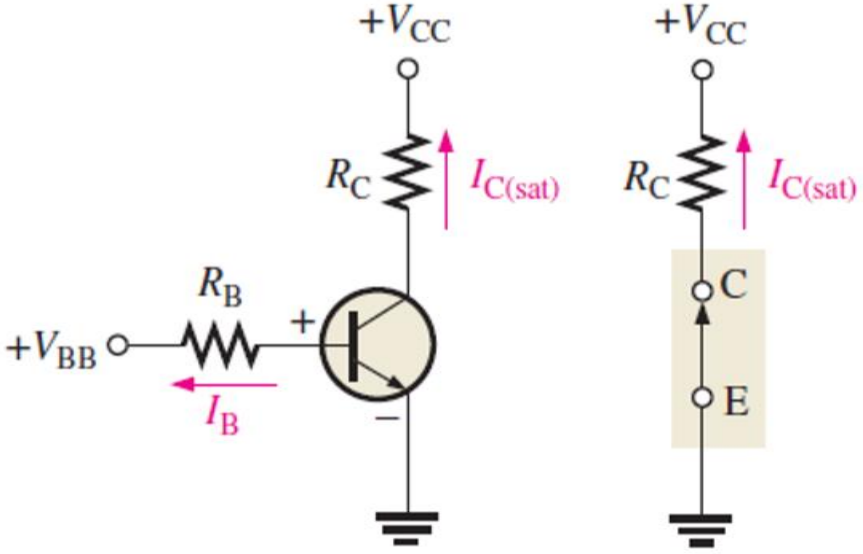
Cut-Off State:



- Considering the transistor in the cutoff region because the base-emitter junction is not forward-biased. In this condition, there is, ideally, an open between collector and emitter, as indicated by the switch equivalent.
- Neglecting leakage current, all of the currents are zero, and V_{CE} is equal to V_{CC}.

$$\mathbf{V_{CE(CUTOFF)} = V_{CC}}$$

Saturation State:



- Considering the transistor in the saturation region, because the base emitter junction and the base-collector junction are forward-biased and the base current is made large enough to cause the collector current to reach its saturation value.
- In this condition, there is, ideally, a short between collector and emitter, as indicated by the switch equivalent.
- Actually, a small voltage drop across the transistor of up to a few tenths of a volt normally occurs, which is the saturation voltage, $V_{CE(sat)}$.
- The formula for collector saturation current is:

$$I_{C(SAT)} = \frac{V_{CC} - V_{CE(SAT)}}{R_C}$$

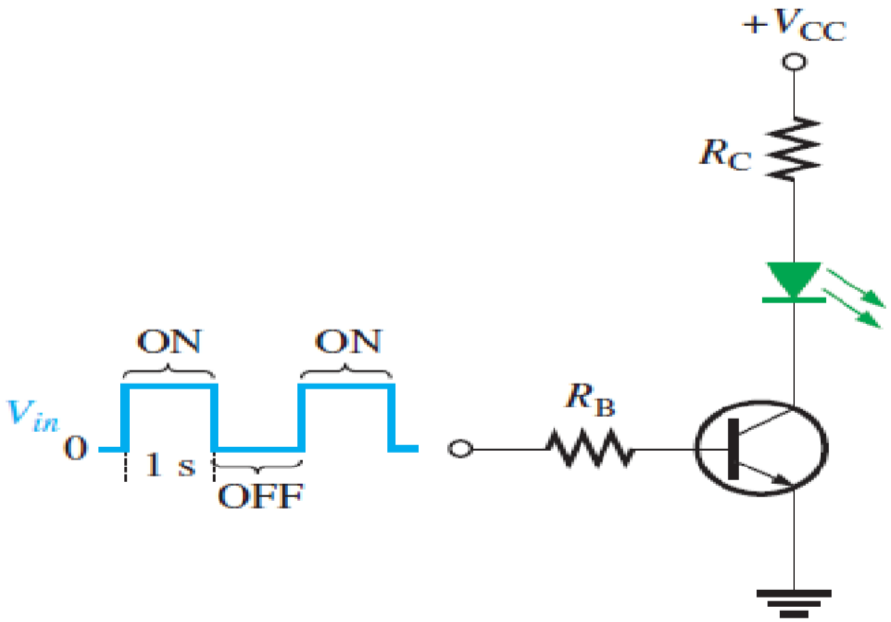
- Since $\mathbf{V_{CE(sat)}}$ is very small compared to $\mathbf{V_{CC}}$, it can be neglected.
- The minimum value of base current needed to produce saturation is

$$I_{B(\min)} = \frac{I_{C(SAT)}}{\beta_{DC}}$$

- Normally, I_B should be significantly greater than $\mathbf{I_{B(min)}}$ to ensure that the transistor is saturated.

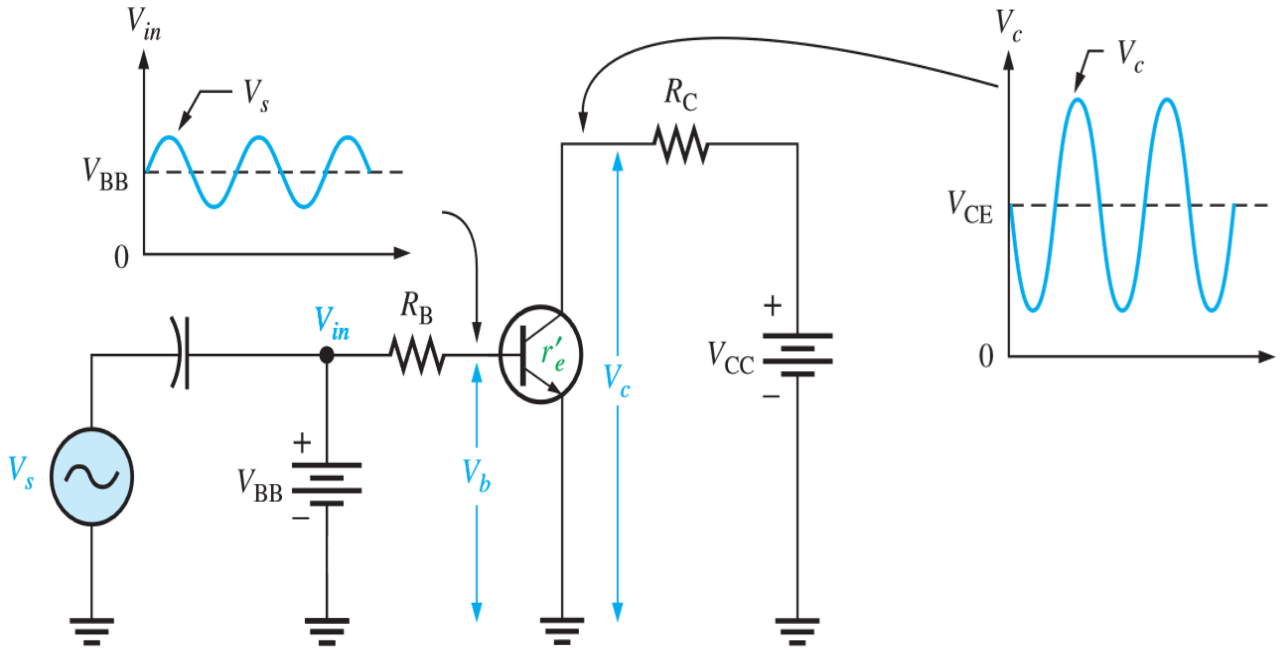
A Simple Application of a Transistor Switch to turn ON LED:

- The transistor in figure below is used as a switch to turn the LED on and off. For example, a square wave input voltage with a period of 2 s is applied to the input as indicated.
- When the square wave is at 0 V, the transistor is in cut-off; and since there is no collector current, the LED does not emit light.
- When the square wave goes to its high level, the transistor saturates. This, forward-biases the LED, and the resulting collector current through the LED cause it to emit light.
- Thus, the LED is on for 1 second and off for 1 second.



BJT as an Amplifier:

- BJT's in Active region is used as an Amplifier.
- **Transistor amplifies current, output current is gain times of controlling current i.e. $I_C = \beta * I_B$**
- The circuit connection of the BJT used as an amplifier is as shown below.



- An AC voltage V_S is applied with the DC bias voltage V_{BB} by capacitor coupling to the Base of the transistor through base resistor R_B.
- DC bias voltage V_{CC} is applied to the collector through collector resistor R_C.
- The AC input voltage make base-emitter junction forward biased which produces base current I_B, which results in larger collector current I_C.
- Thus I_C produces AC voltage across R_C which produces an amplified and inverted output as shown in the figure.
- The AC base voltage V_B is given by:

$$V_B = I_E * r'_E$$

- The AC collector voltage V_C across R_C is given by:

$$V_C = I_C * R_C$$

- Since $I_C \cong I_E$
- V_B is an input voltage given by $V_B = V_S - I_B * R_B$.
- V_C is an output voltage.
- Voltage gain A_V is defined by:

$$A_V = \frac{V_C}{V_B} = \frac{I_C * R_C}{I_E * r'e} \cong \frac{I_E * R_C}{I_E * r`_E}$$

$$A_V \cong \frac{R_C}{r`_E}$$

Thus the above equation shows that the transistor provides amplification in the form of voltage gain.

Feedback Circuits:

The feedback-amplifier can be defined as an amplifier which has feedback line that exists between output to input.

- In amplifier, feedback is the limitation which calculates the sum of feedback given in the amplifier.
- Feedback is mainly used to reduce the noise as well as to make the operation of an amplifier is constant.
- Feedback amplifier can be classified into two types based on the feedback signal, such as positive & negative feedback amplifier.

Positive Feedback Amplifier:

- The positive feedback can be defined as when the feedback current or voltage is applied for increasing the input voltage.
- Direct feedback is another name of this positive feedback. Because positive feedback generates unnecessary distortion; it is not often used in amplifiers. But, it amplifies the original signal power and can be used in oscillator circuits.

Negative Feedback Amplifier:

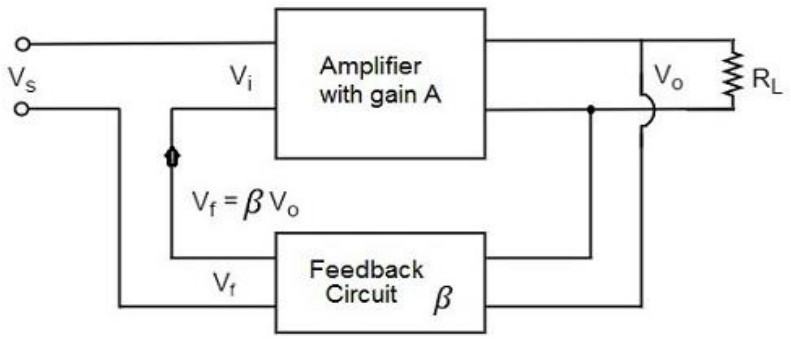
- The negative feedback can be defined as if the feedback current or voltage can be applied for reducing the amplifier input, then it is called as negative feedback.
- Inverse feedback is another name of this negative feedback. This kind of feedback is regularly used in amplifier circuits.

There are *four basic amplifier topologies* for connecting the feedback signal. Both the current as well as voltage can be feedback toward the input in series otherwise in parallel.

1. Voltage Series feedback amplifier
2. Voltage Shunt feedback amplifier
3. Current Series feedback amplifier
4. Current Shunt feedback amplifier

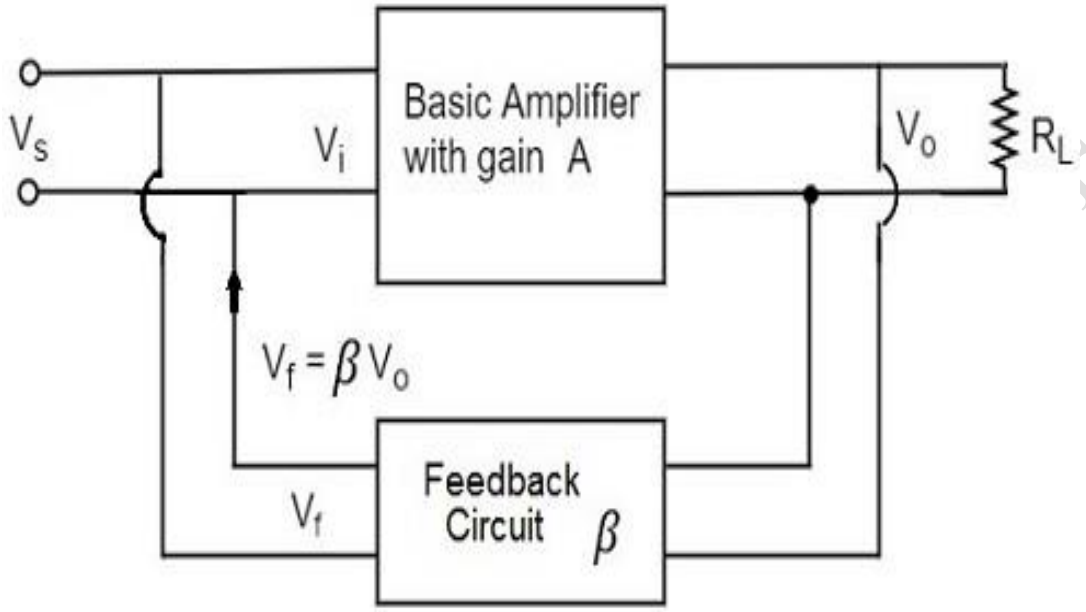
***Voltage Series Feedback Amplifier*:**

- In this type of circuit, a portion of the o/p voltage can be applied to the input voltage in series through the feedback circuit.
- The block diagram of the voltage series feedback-amplifier is shown below, by which it is apparent that the feedback circuit is located in shunt by means of the output although in series by means of the input.
- When the feedback circuit is allied in shunt through the output, then the ***output impedance*** will be ***reduced*** and the ***input impedance*** is ***increased*** because of the series connection with the input.



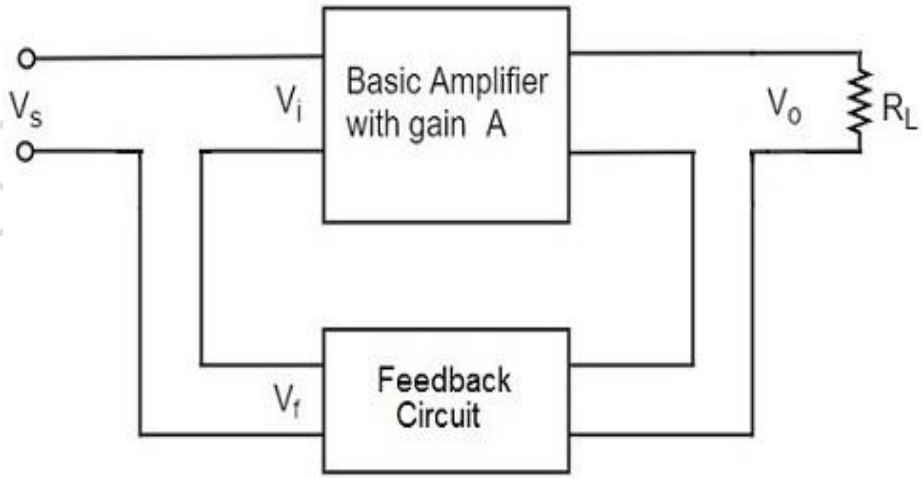
***Voltage Shunt Feedback Amplifier*:**

- In this type of circuit, a portion of the output voltage can be applied to the input voltage in parallel with through the feedback circuit.
- The block diagram of the voltage shunt feedback-amplifier is shown below, by which it is apparent that the feedback circuit is located in shunt by means of the output as well as the input.
- When the feedback circuit is allied in shunt through the output as well as the input, then both the ***output impedance & the input impedance will be decreased***.



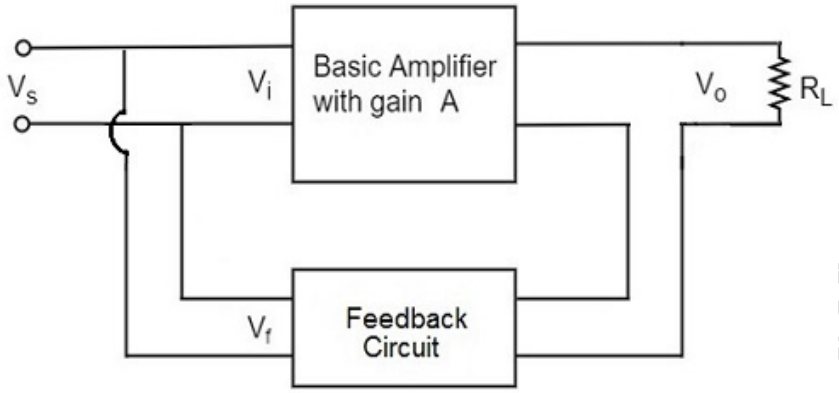
***Current Series Feedback Amplifier*:**

- In this type of circuit, a portion of the o/p voltage is applied to the input voltage in series through the feedback circuit.
- The block diagram of the current series feedback-amplifier is shown below, by which it is apparent that the feedback circuit is located in series by means of the output as well as the input.
- When the feedback circuit is allied in series through the output as well as the input, ***then both the output impedance & the input impedance will be increased***.



***Current Shunt Feedback Amplifier*:**

- In this type of circuit, a portion of the o/p voltage is applied to the input voltage in shunt through the feedback circuit.
- The block diagram of the current shunt feedback-amplifier is shown below, by which it is apparent that the feedback circuit is located in shunt by means of the output as well as the input.
- When the feedback circuit is allied in series through the o/p however in parallel with the input, then the output impedance will be increased & because of the parallel connection with the input, the ***input impedance*** will be ***decreased***.

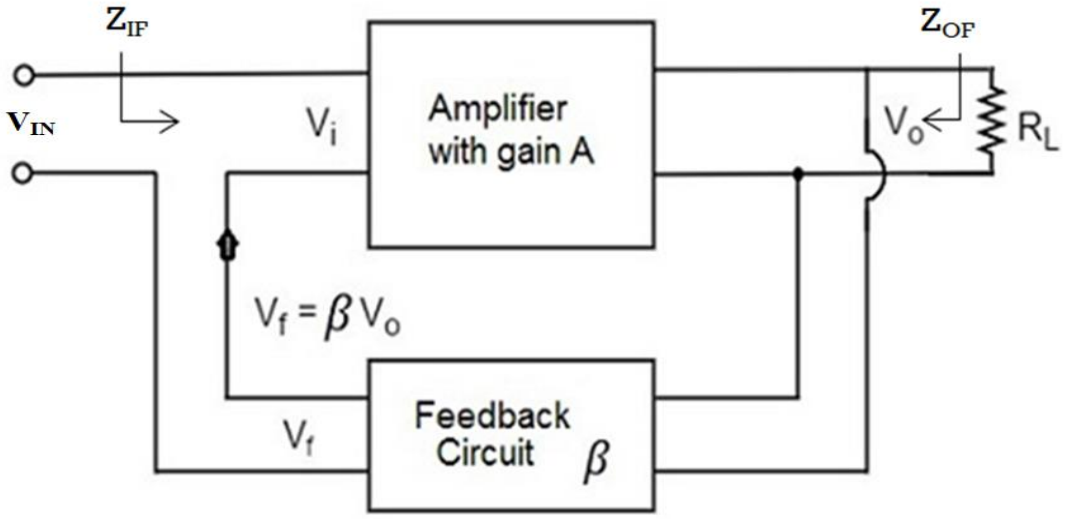


The advantages of this amplifier include the following:

1. The amplifier's gain can be stabilized by the negative feedback.
2. The particular feedback configurations can be increased by the input resistance.
3. Output resistance will be decreased for particular feedback configurations.
4. The operating point is stabilized.

Voltage Series:

Considering the voltage series feedback which is called as Series-Parallel feedback is shown in the below figure. Here the feedback is negative.



From the figure,

$\mathbf{V_i = V_{in} - \beta V_o}$

$\mathbf{V_o = AV_i = A\,(V_{in} - \beta V_o) = A*V_{in} - A*\beta*V_o}$

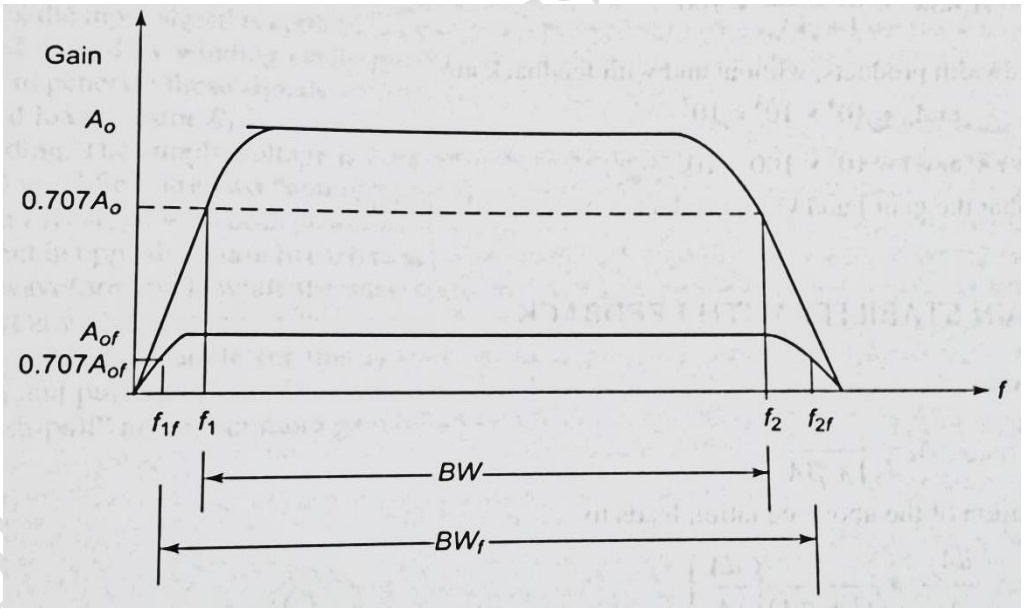
Gain with feedback equation is as follows which is applicable to all types of feedback circuits.

$$\frac{V_o}{V_{in}} = A_F = \frac{A}{1+\beta A}$$

1. The amplifier gain reduces by a factor of $(1 + \beta A)$.
2. Input impedance with feedback, $Z_{if} = Z_i (1 + \beta A)$ increases and output impedance with feedback, $Z_{of} = Z_o/(1 + \beta A)$ decreases.
3. If $\beta A \gg 1$then A_F is given by $A_F = \frac{1}{\beta}$
4. From the above equation we can conclude that feedback gain is independent of amplifier gain A.
5. Any variation in magnitude of A does not appear in A_F, which means A_F has high gain stability.

Gain and Bandwidth of Feedback Amplifier:

1. We know that negative feedback reduces the amplifier gain, and hence it increase its bandwidth.
2. In RC – coupled amplifiers, the gain reduces at low frequency and high frequency ends. So βA_o is no longer much more than unity.
3. As a result, the percent reduction in gain is less at the two frequency ends compared to the mid-band.
4. The reduction in gain and increases in bandwidth of feedback amplifier is as shown below:



As $f_1 \ll f_2$ and $f_{1f} \ll f_{2f}$ therefore,

$BW = f_2$;

$BW_f = f_{2f}$

It can be shown that, $A_o f_2 = A_o f_{2f}$ = constant product of gain bandwidth.

Gain Stability with feedback:

Overall gain with negative feedback is $A_F = \frac{A}{1+\beta A}$

Differentiation of above equation gives:

$$\frac{dA_f}{A_f} = \frac{1}{1+\beta A}\left(\frac{dA}{A}\right);$$

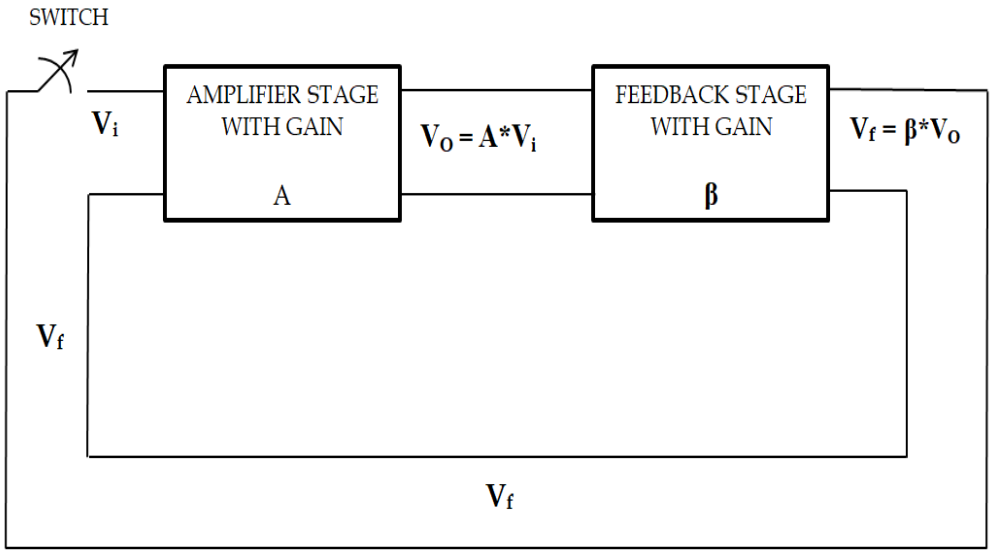
$$\frac{dA_f}{A_f} = \frac{1}{\beta A}\left(\frac{dA}{A}\right) = \text{for } \beta A \gg 1$$

This shows that a relative change (dA/A) in the basic amplifier gain is reduced by the factor of βA in the relative change (dA_f/A_f) in the overall gain of the feedback amplifier.

Oscillator Operation and Barkhausen Criterion:

- The use of positive feedback that results in a feedback amplifier having closed loop gain $|\mathbf{A_f}|$ greater than Unity (1) and satisfies the phase condition will result in operation as an Oscillator circuit.
- An oscillator circuit generates oscillations with the feedback circuit, without any input which will be of constant amplitude and frequency.
- If the output signal varies sinusoidal with time, the circuit id referred to as a "Sinusoidal Oscillator".
- If the output voltage rises quickly to one voltage level and later drops quickly to another voltage level, the circuit is generally referred to as "Pulse or Square Wave Oscillator".

Barkhausen Criterion:



- Consider a basic inverting amplifier with an gain **A** and the feedback netwrok gain **β**.
- The input $\mathbf{V_i}$ is applied to the Amplifier through a switch whose output is $\mathbf{V_O}$ which is 180^o phase shifted output. This will be fed as input to the feedback stage whose output is $\mathbf{V_f}$.
- When the switch is closed, the input $\mathbf{V_i}$ is applied to the amplifier.

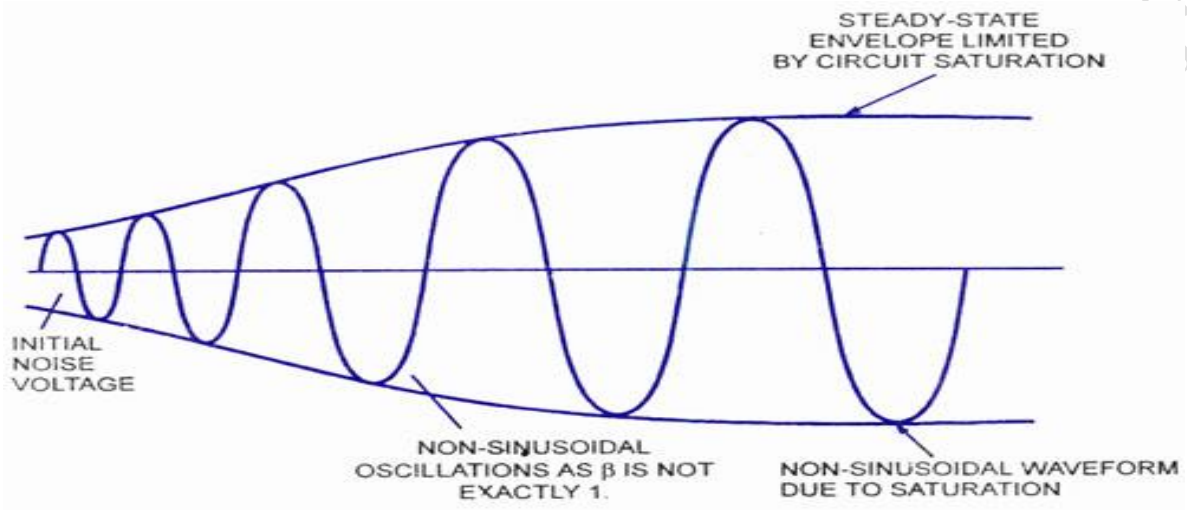
$$\mathbf{V_O = A*V_i}$$

- For an oscillator, the output of the feedback circuit should drive the amplifier stage, so $\mathbf{V_f}$ should be equal to $\mathbf{V_i}$. Hence for $\mathbf{V_f}$ to be inphase with $\mathbf{V_i}$ feedback circuit should produce 180^o phase shift.

$$\mathbf{V_f = \beta * V_O}$$

$$\mathbf{V_f = A * \beta * V_i}$$

- When the switch is closed and the input voltage $\mathbf{V_i}$ is stopped, the output voltage of feedback circuit $\mathbf{V_f}$ should drive the amplifier producing continuous output.
- For this to happen, $|\mathbf{\beta A}| = 1$, so that $\mathbf{V_f = V_i}$.
- This condition is called as ***Barkhausen Criteria***.



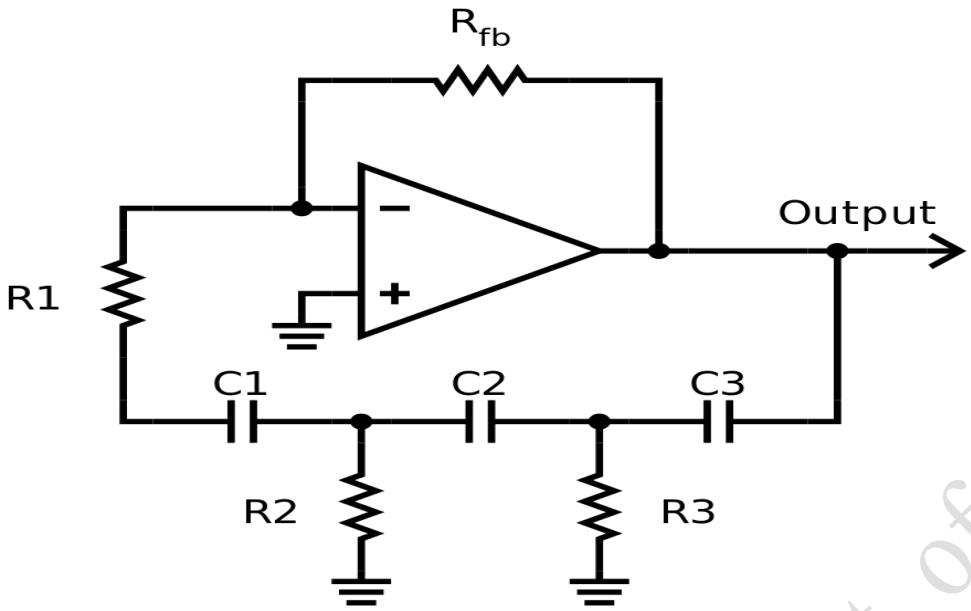
Phase Shift Oscillator:

- An oscillator circuit that follows the basic development of a feedback circuit is the Phase Shift Oscillator.
- RC phase shift oscillator basically consists of an Amplifier and a feedback circuit.
- Feedback circuit consists of a resistor and a capacitor (**RC**) connected in parallel.
- Feedback circuit should produce phase shift of 180^0.
- One RC component produces phase shift of 60^0. So to get180^0 phase shift, we need to use 3 RC components which are connected in series.
- Hence in RC Phase Shift Oscillator circuit, feedback circuit consists of 3 RC components.
- The output of the amplifier is given to feedback network. The output of the feedback circuit drives the amplifier.
- We find the frequency of the oscillator which is dependent on the values of R and C is given by;

$$\boldsymbol{f = \frac{1}{2\pi RC\sqrt{6}}}$$

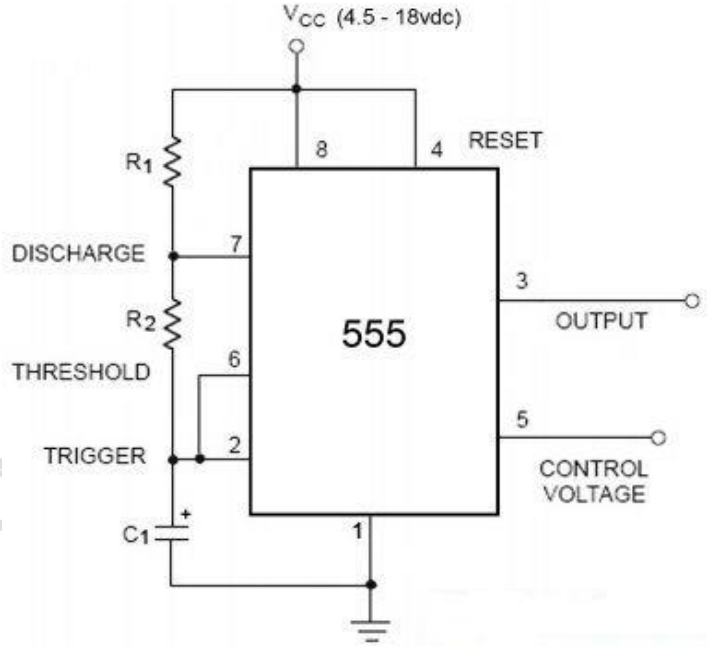
and feedback gain $\mathbf{\beta}$ is $\frac{\mathbf{1}}{\mathbf{29}}$

- For loop gain (βA) to be greater than Unity. Gain of the amplifier stage (A) must be greater than $\frac{\mathbf{1}}{\boldsymbol{\beta}}$ or 29. Hence A = 29
- An RC Phase Shift Oscillator with an Op-Amp is as shown below

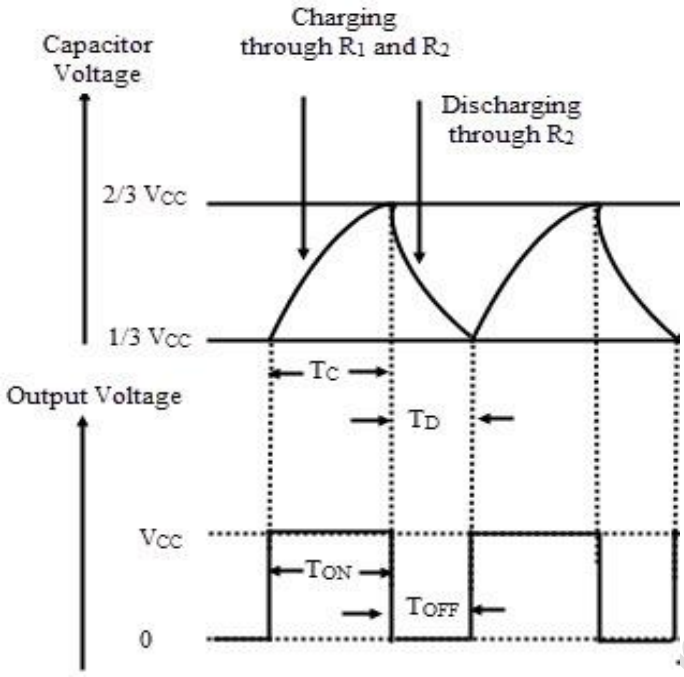


Astable Operation:

1. One of the main applications of 555 timers is as astable multivibrator or clock circuit.
2. Figure below shows astable circuit built using two external resistors and a capacitor, which sets the timings in interval of the output.



3. The capacitor begins to charge from the DC source V_{CC}, when the voltage of the threshold pin 6tends to increase beyond 2/3 V_{CC}, the comparator 1 saturates and its output triggers the flip-flop and so the output at pin 3 goes low.
4. At the same time, the transistor becomes 'On' causing the output at pin 7 to discharge the capacitor through R_2 at time constant =R_2C.
5. As the capacitor voltage which is the trigger input at pin 2 falls below 1/3 V_{CC}, the comparator 2 output causes the flip-flop to reset, the output at pin 3 becomes high and the transistor goes 'Off'.
6. The capacitor begins to charge through R_1 and R_2 at the time constant = $(R_1+R_2)C$. The process then repeats continuously.
7. The output waveform and the capacitor charging and discharging are as shown below:



8. The charging time and the discharging time is given by T_{High} and T_{Low} which is given by equations:
   $T_{High} = 0.7(R_1+R_2)C$
   $T_{Low} = 0.7\ R_2C$
   The oscillator period: **$T = T_{High} + T_{Low}$**
   The oscillator frequency: $f = \frac{1}{T} = \frac{1.44}{(R_1+2R_2)C}$
9. Duty cycle is less than 50%.

MODULE 5

DIGITAL ELECTRONICS AND COMMUNICATION SYSTEMS

Difference between Digital Signal and Analog Signal:

Analog Signal	Digital Signal
An analog signal is a continuous wave that changes over a time period.	A digital signal is a discrete wave that carries information in binary form.
An analog signal is represented by a sine wave.	A digital signal is represented by a square waves.
An analog signal is described by the amplitude, period or frequency and phase.	A digital signal is described by the bit rate and bit intervals.
An analog signal has no fixed range.	Digital signal has a finite range i.e. between 0 and 1.
An analog signal gets more infected to distortion.	A digital signal is less infected to distortions.
An analog signal transmits data in the form of a wave.	A digital signal carries data in the binary form.
Eg: Human Voices, Musical Instrument Sounds	Eg: Signals used for transmission in the Computer.

Number System:

- There are many types of numbering systems to represent the numerals.
- Here we are studying
    1. Binary
    2. Decimal
    3. Hexadecimal
- Usually number systems are classified based on its ***"Radix Number"*** or ***"Base Numbers"***.
- Radix number for:
    1. **Binary is '2' = ( )$_2$**
    2. **Decimal is '10' = ( )$_{10}$**
    3. **Hexadecimal is '16'= ( )$_{16}$**

1. **Binary Number System:**
    - These are represented by **'Radix'** or **'Base' 2.**
    - These consist of 0's and 1's.
    - Binary digits are also called 'Bits'.

2. **Decimal Number System:**
    - These are represented by Radix or Base 10
    - It consists of numerals from 0 – 9.

3. **Hexadecimal Number System:**
    - These are represented by Base or Radix 16.
    - It consists of numerals from 0 – 15.
    - Numerals 10,11,12,13,14,15 are represented by A,B,C,D,E,F respectively called as Alpha-numerals.

Boolean algebra Theorems:

A Boolean algebra is a set of binary operations, + and *, and a unary operation, '-' and elements such as 0,1 such that the following laws hold: Commutative and Associative Laws for addition and subtraction, Distributive law for both Addition over Multiplication and Multiplication over Addition.

The application of digital logic involve functions of the AND, OR and NOT operations.

1. AND – Multiplication Symbol (**.**):

   Y = A AND B = A **.** B

A	B	Y
0	**0**	**0**
0	**1**	**0**
1	**0**	**0**
1	**1**	**1**

2. OR – Addition Symbol (+):

   Y = A OR B = A + B

A	B	Y
0	**0**	**0**
0	**1**	**1**
1	**0**	**1**
1	**1**	**1**

3. NOT – Complement, Symbol (A):

   Y = NOT (A) = $\overline{A}$

A	Y
0	**1**
1	**0**

Conversions :-

1. Binary to Decimal :-

→ Decimal equivalent of a binary number is formed by multiplying each bit in the binary number by the binary radix of 2 raised to the positions power.

→ The result of each multiplication is expressed as a decimal number.

→ The individual decimal numbers are added to obtain the decimal equivalent of the binary number.

Eg:- 1. $(111110100)_2 = (\quad)_{10}$

Binary Number ↑ 2 — Decimal Number ↑ 10

1 1 1 1 1 0 1 0 0

8^{th} 7^{th} 6^{th} 5^{th} 4^{th} 3^{rd} 2^{nd} 1^{st} 0^{th} → position

2 ↑ position

$\Rightarrow 1\times2^8 + 1\times2^7 + 1\times2^6 + 1\times2^5 + 1\times2^4 + 0\times2^3 + 1\times2^2 + 0\times2^1 + 0\times2^0$

$= 256 + 128 + 64 + 32 + 16 + 0 + 4 + 0 + 0$

$= (500)_{10}$ ⇒ Decimal Equivalent

For Fractions :-

Eg:- 2. $(11101011 \cdot 1011)_2 = (\quad)_{10}$

positions → 7 6 5 4 3 2 1 0 (-1)(-2)(-3)(-4)

$\Rightarrow 1\times2^7 + 1\times2^6 + 1\times2^5 + 0\times2^4 + 1\times2^3 + 0\times2^2 + 1\times2^1 + 1\times2^0 + 1\times2^{-1} + 0\times2^{-2} + 1\times2^{-3} + 1\times2^{-4}$

$= 128 + 64 + 32 + 0 + 8 + 0 + 2 + 1 + 0.5 + 0 + 0.125 + 0.0625$

$= (235.6875)_{10}$

2] Binary to Hexadecimal :-

→ Binary numbers are converted to hexadecimal numbers by dividing the binary number into group of 4-bits. [Starting at the LSB & grouping to the left]

→ To make a 4-bits, we can add zeroes to the leftmost bits.

Eg:-1. $(1111\,0100)_2 = (\quad)_{16}$

added 3 zeroes to group → 0001

∴ ⇒ 0001 1111 0100

1 15 4 ⇒ Decimal

$= (1F4)_{16}$ ⇒ Hexadecimal

Eg:- 2.

$(1101\,1100 \cdot 1001)_2 = (\quad)_{16}$

13 12 9

$= (DB \cdot 9)_{16}$

Hexa Numbers	Binary	Decimal Numbers
0	0000	0
1	0001	1
2	0010	2
3	0011	3
4	0100	4
5	0101	5
6	0110	6
7	0111	7
8	1000	8
9	1001	9
A	1010	10
B	1011	11
C	1100	12
D	1101	13
E	1110	14
F	1111	15

→ Hexadecimal & Decimal numbers 0 to 9 are same.

3] Decimal to Binary :-

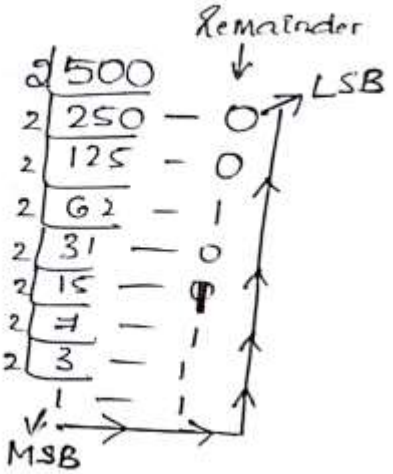
→ Conversion of decimal number to binary number is done by Repeated division of the decimal number by the binary Radix of 2.

→ The decimal number is Repeatedly divided by 2, and the remainder becomes the bits of the equivalent binary number.

→ The remainder of the first division operation yields the Least Significant Bit [LSB] & the final remainder is the Most Significant Bit [MSB].

Eg:- 1. $(500)_{10} = (\quad)_2$

$(111110100)_2$



Eg:- 2

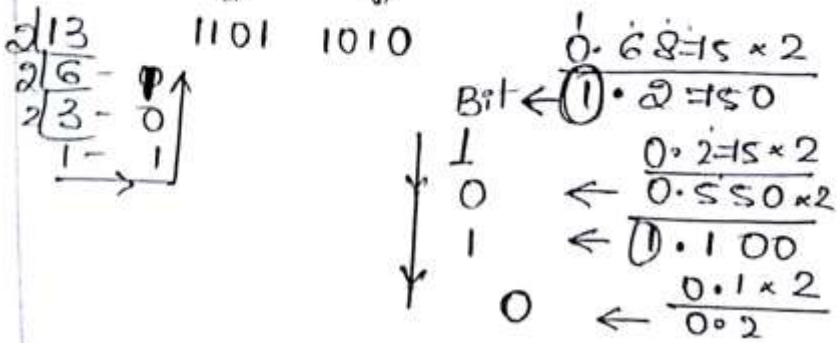
For Fractions :-

→ The numbers after decimal are multiplied by 2, and

→ the carry are considered as bits of the equivalent binary number.

Eg:- 2. $(13.68\overline{=15})_{10} = (\quad)_2 \Rightarrow (1101.1010)$

1101 1010



4] Decimal to Hexadecimal :-

→ Converting a decimal number into a hexadecimal number involves repeated steps of dividing a decimal quotient by radix 16.

→ At each step the decimal remainder is replaced with its equivalent hexadecimal numeral.

→ The remainder of the first division step is the LSB of the hexa number & the remainder of last division step is the MSB.

Eg:- 1. $(356+141)_{10} = (\quad)_{16}$

$(356+141)_{10} = (5+1185)_{16}$

Eg: 2: Fraction Decimal Values :-

$(8899.15)_{10} = (\quad)_{16}$

$(8899.15)_{10} = (22B3.29)_{16}$

16 | 8899
16 | 556 - 3
16 | 34 - 11 → B
2 - 2

0.15 × 16
2 ← 2.50
0.50 × 16
9 ← 9.0

→ For the conversion of fractional decimal no's to Hexa, multiply by 16. If you getting repeated values stop for 4 bits or 4 numerals.

5] Hexadecimal to Binary :-

→ To convert from a hex number to a binary number requires that a 4-bit binary number, which is to be entered in place of each hex numeral

→ Each numeral of the hex number becomes a 4-bit binary number.

Eg:- 1. $(3DEC8FE)_{16} = (\quad)_2$

Hexa number →	3	D	E	C	8	F	E
Binary Equivalent →	0011	1101	1110	1100	1000	1111	1110

$\therefore (3DEC8FE)_{16} = (0011110111101100100011111110)_2$

Eg:- 2. Fractions in Hexa

→ For (decimal) fractions, similarly convert the given hexa numerals into its respective binary equivalent.

$(DFAB \cdot C8E)_{16} = (\quad)_2$

$(1101111110101011 \cdot 110010001110)_2$

Eg:- 3 $(=8A \cdot B89)_{16} = (\quad)_2$

=	8	A	B	8	9
0111	1000	1010	1011	1000	1001

$(=8A \cdot B89)_{16} = (0111\ 1000\ 1010 \cdot 1011\ 1000\ 1001)_2$

6] Hexadecimal to Decimal :-

→ Conversion from hex to decimal is begun by converting each hex numeral of the hex number into the decimal equivalent [i.e A→10, B-11, ... F-15].

→ Each decimal number is then multiplied by hex radix ie 16 raised to its position power.

Eg:-1 $(5DECA)_{16} = (\quad)_{10}$

(4 3 2 1 0)

$5\times16^4 + D\times16^3 + E\times16^2 + C\times16^1 + A\times16^0$

$5\times16^4 + 13\times16^3 + 14\times16^2 + 12\times16 + 10\times1$

$= 5\times65536 + 13\times(4096) + 14\times256 + 12\times16 + 10$

$= 327680 + 53248 + 3584 + 192 + 10$

$= (384714)_{10}$

Eg:- 2. Fractions

$(3E\cdot4FC)_{16} = (\quad)_{10}$

(1 0 -1 -2 -3)

$(3E\cdot4FC)_{16} = 3\times16^1 + E\cdot16^0 + 4\times16^{-1} + F\times16^{-2} + C\times16^{-3}$

$= 3\times16 + 14\times1 + \frac{4}{16} + \frac{15}{16^2} + \frac{12}{16^3}$

$= 48 + 14 + 0.25 + 0.05859375 + 0.00292968$

$(3E\cdot4FC)_{16} = (62.31152343375)_{10}$

Binary Addition & Binary Subtraction:

→ There are four possible results when two binary numerals are added together & one numeral is subtracted from the other.

→ Addition of two binary numerals may have one of the four results shown below.

(i) Carry 1] 1 add 1 = 1] 0

(ii) Carry 0] 1 + 0 = 0] 1 (Carry ↓)

(iii) Carry 0] 0 + 1 = 0] 1 (Carry ↓)

(iv) Carry 0] 0 + 0 = 0

→ Carries are shown using a parenthesis [brackets] to indicate the carry bit.

Eg:- 1

$$\begin{array}{rl} 95 = & 0\,1\,0\,1\,1\,1\,1\,1 \\ \text{add } 189 = & 0\,1\,0\,1\,1\,1\,0\,1 \\ \hline 284 & 1\,]\,0\,0\,0\,1\,1\,1\,0\,0 \end{array}$$

Carry ↓

$\Rightarrow 256 + 28 = 284$

→ Subtraction of two binary numerals may have one of the four results shown below.

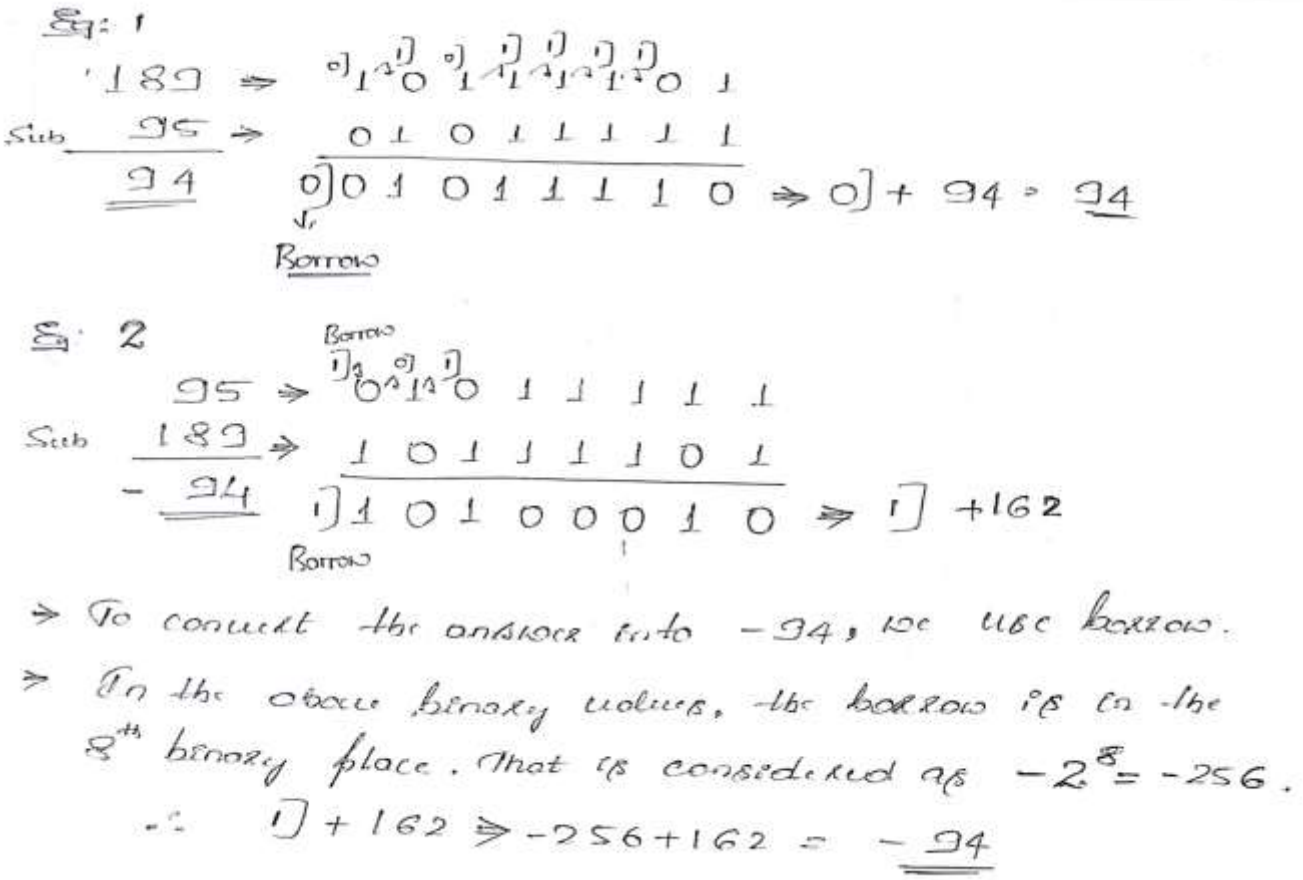
(i) Borrow ↓ 0] 1 Sub 1 = 0

(ii) Borrow 1] 0 Sub 1 = 1

(iii) Borrow 0] 1 − 0 = 1

(iv) Borrow 0] 0 − 0 = 0

IMP → When we borrow a bit i.e 1, the number becomes 10 whose decimal equivalent is 2.



Binary Subtraction using Two's compliment form:

Consider the case [m – n], For two's complimentary subtraction:

1. Take the two's compliment of the Subtrahend 'n', then add the 'n' two's compliment with the minuend 'm'
2. If the sum has a carry at the left end, delete it. The answer is (m - n).
3. If the sum has no carry at the left end, take 2's compliment of the sum. Attach the negative sign. The result is (m - n).

Example:

Given: **m = 11001010 n = 11010110**
Perform: 1. m – n 2. n - m

1. m – n = m + n(2's)

n 1's 00101001
\+ 1
00101010

m + n (2's) 11001010
\+ 00101010
NO Carry 11110100 → SUM

Hence we take 2's compliment of the Sum and attach negative sign

11110100
1's 00001011
\+ 1

m – n = - (00001100)

2. n - m = n + m(2's)

m 1's 00110101
\+ 1
00110110

n + m (2's) 11010110
\+ 00110110
Carry ← **1** 00001100 SUM

Since there is a carry bit, the answer is positive. Neglecting the carry bit, we get answer:

n – m = (00001100)

Simplify or factorise the given Boolean equations:

1. Y = $\bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C}D + A\bar{B}\bar{C}\bar{D} + A\bar{B}\bar{C}D$
2. Y = (B + CA) (C + $\bar{A}B$)
3. Y = $\bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC$
4. Y = AB + AC + BD + CD

Some identities of Boolean Algebra:

NAME	**AND** form	**OR** form
Identity Law	1.A = A	0+A = A
Null Law	0.A = A	1+A = 1
Idempotent Law	A.A = A	A+A = A
Inverse Law	A. $\bar{A}$ = 0	A+$\bar{A}$ = 1
Commutative Law	A.B = B.A	A+B = B+A
Associative Law	(A.B).C = A.(B.C)	(A+B)+C = A+(B+C)
Distributive Law	A+BC = (A+B) . (A+C)	A(B+C)= AB + AC
Absorption Law	A.(A+B) = A	A+AB = A
De Morgan's Law	$\overline{A.B} = \bar{A} + \bar{B}$	$\overline{A+B} = \bar{A}.\bar{B}$

De Morgan's Theorem:

i. $\overline{A.B} = \bar{A} + \bar{B}$ **and** **ii.** $\overline{A+B} = \bar{A}.\bar{B}$

Truth Table to prove De Morgan's Theorems

A	**B**	$\bar{A}$	$\bar{B}$	$\overline{A.B}$	$\bar{A} + \bar{B}$	$\overline{A+B}$	$\bar{A}.\bar{B}$
0	0	1	1	1	1	1	1
0	1	1	0	1	1	0	0
1	0	0	1	1	1	0	0
1	1	0	0	0	0	0	0

Column 5 is same as column 6 which proves $\overline{A.B} = \bar{A} + \bar{B}$

Column 7 is same as column 8 which proves $\overline{A+B} = \bar{A}.\bar{B}$

Digital Circuits:

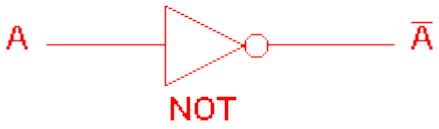
- Digital circuits are classified into two major categories: Combinational Circuits and Sequential Circuits.
- Combinational Circuit are the circuits where output depends on the present input only.
- The sequential circuit produces the output on the basis of the both present and previous inputs.

Logic Gates:

- Logic Circuits are the building blocks of digital circuits. They are used to create digital circuits and even complex integrated circuits.
- Logic Gates are classified as Basic Gates and Universal Gates.
- Basic gates are AND, OR and NOT.
- Universal gates are NAND, NOR.

1. NOT Gate:

- NOT gate is also known as inverter, because it inverts the input to its opposite.
- The NOT gate accepts one input and the Output is the opposite of the input as shown in figure below and the Truth Table is as soon below.



NOT gate	
A	$\overline{A}$
0	1
1	0

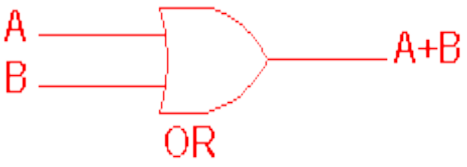
2. AND Gate:

- It performs logical AND operation, which is logic multiplication.
- It has atleast Two inputs. If A and B are inputs, at the output we will find Y = A . B.
- When both the inputs are '1', output is '1' and when either of the input is '0' output is '0'.
- The logical symbol and truth table is as shown below.

2 Input AND gate		
A	B	A.B
0	0	0
0	1	0
1	0	0
1	1	1

3. OR Gate:

- It performs logical OR operation, which is logic addition.
- It has atleast two inputs. If A and B are inputs, at the output we will find Y = A + B.
- When both the inputs are '0', output is '0' and when either of the input is '1' output is '1'.
- The logical symbol and truth table is as shown below.



2 Input OR gate		
A	B	A+B
0	0	0
0	1	1
1	0	1
1	1	1

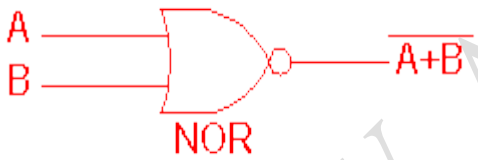
4. NAND Gate:

- This is an AND gate with the output inverted.
- The output is Low (0) when both of the inputs A & B is High (1).
- Output is High (1) when either of the input A or B is (0).
- In other words, it is high, going low only if both A and B is high.
- Its symbol and truth table is as shown below.

2 Input NAND gate		
A	B	$\overline{A.B}$
0	0	1
0	1	1
1	0	1
1	1	0

5. NOR Gate:

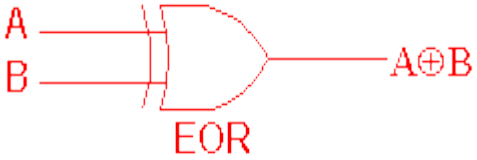
- This is an OR gate with the output inverted.
- The output is High (1) when both of the inputs A & B are Low (0).
- Output is Low (0) when either of the input is High (1).
- In other words, it is high, going low only if both A and B is high.
- The logical symbol and truth table is as shown below.



2 Input NOR gate		
A	B	$\overline{A+B}$
0	0	1
0	1	0
1	0	0
1	1	0

6. XOR Gate:

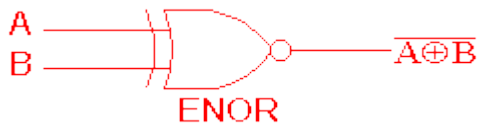
- XOR stands for Exclusive-OR.
- An XOR gate produces output '1' when either of the input is '1'.
- When both inputs are either Low '0' or High '1', output will be Low '0'.
- It is represented by the symbol ''.
- The output Y = A⊕B.
- The logical symbol and truth table is as shown below.



2 Input EXOR gate		
A	B	A⊕B
0	0	0
0	1	1
1	0	1
1	1	0

7. XNOR Gate:

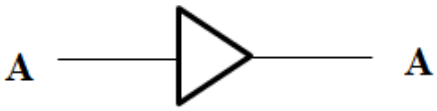
- XOR stands for Exclusive-OR.
- An XOR gate produces output '1' when either of the input is '1'.
- When both inputs are either Low '0' or High '1', output will be Low '0'.
- It is represented by the symbol 'Θ'.
- The output Y = A Θ B. [Can be written as $\overline{A \oplus B}$]
- The logical symbol and truth table is as shown below.



2 Input EXNOR gate		
A	B	$\overline{A \oplus B}$
0	0	1
0	1	0
1	0	0
1	1	1

8. Non-Inverter or Buffer:

- At a non-inverter, also known as a buffer, the value entered on its input will be found on its output.
- A typical application for a buffer is to increase the Fan-out of a given logic gate.
- Fan-out is the maximum number of gates a given integrated circuit is capable of being connected to.



A	Y
0	0
1	1

Realization of Gates using NAND only

1. AND
2. OR
3. NOT
4. NOR

Realization of Gates using NOR only

1. AND
2. OR
3. NOT
4. NAND

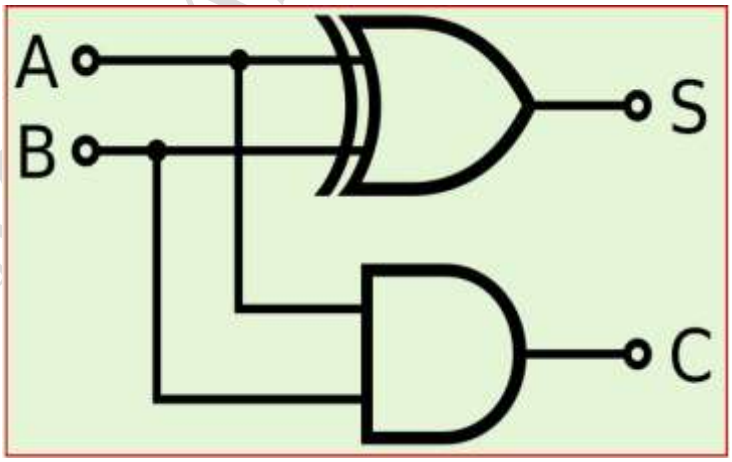
ADDER:

- Adders are the logical circuit which adds two or more binary bits whose outputs are **Sum** and **Carry**.
- The least significant bit produces Sum and most significant bit produces Carry.
- It is classified into two types:
  1. **Half Adder**
  2. **Full Adder**

HALF ADDER:

- Half adder is an example of a simple functional circuit built from two logic gates.
- The half adder adds two one-bit binary numbers (A, B).
- The output is the SUM (S) of the two input bits and the Carry (C).
- The below figure shows the schematic of half adder circuit.

INPUTS		OUTPUTS	
A	B	SUM	CARRY
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1



Expressions for Sum and Carry:

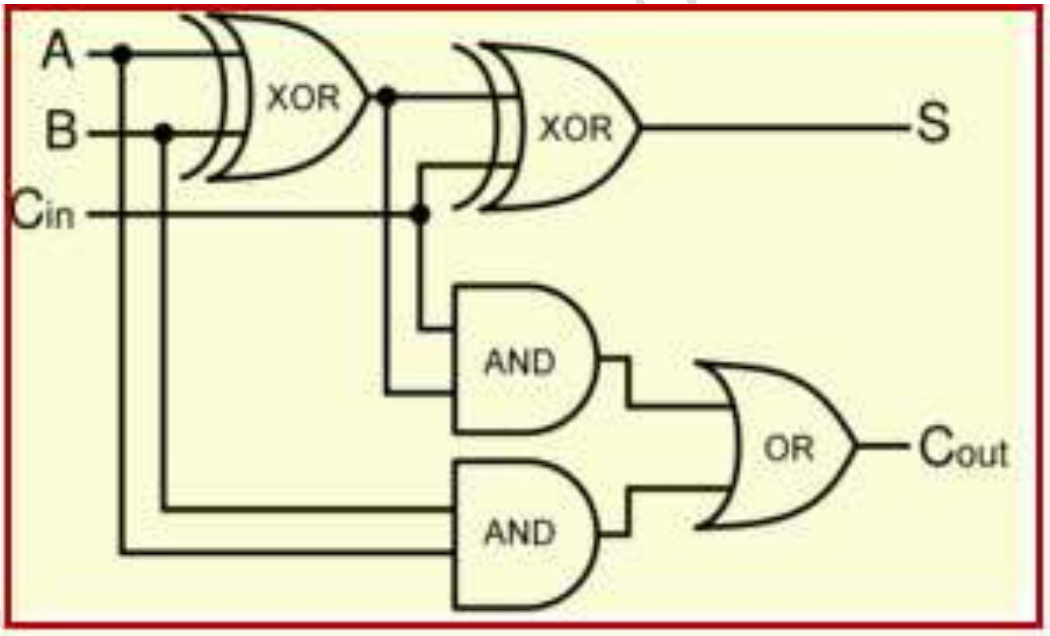
Sum $= \bar{A}B + A\bar{B} = A \oplus B$

Carry $= AB$

FULL ADDER:

- Full adder adds three one-bit binary numbers (A, B, C_{in}).
- The one output is the SUM (S) of the three input bits and the Carry (C_{out}).
- The below figure shows the schematic of full adder circuit.

INPUTS			OUTPUT	
A	B	C-IN	C-OUT	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1



Expression for Sum and Carry:

Sum $= \bar{A}\bar{B}C_{in} + \bar{A}B\overline{C_{in}} + A\bar{B}\overline{C_{in}} + ABC_{in}$

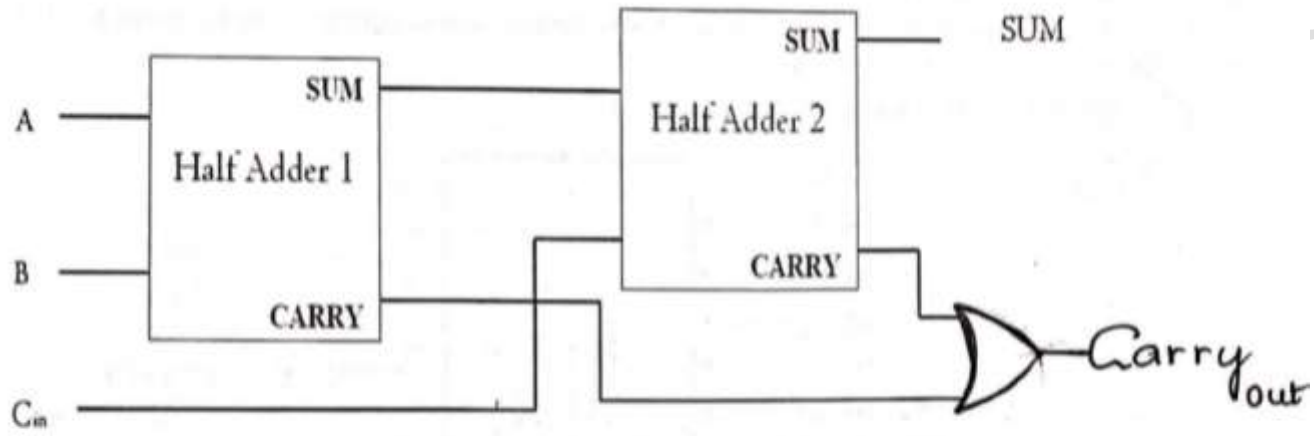
$= A \oplus B \oplus C_{in}$ *(Simplified final expression)*

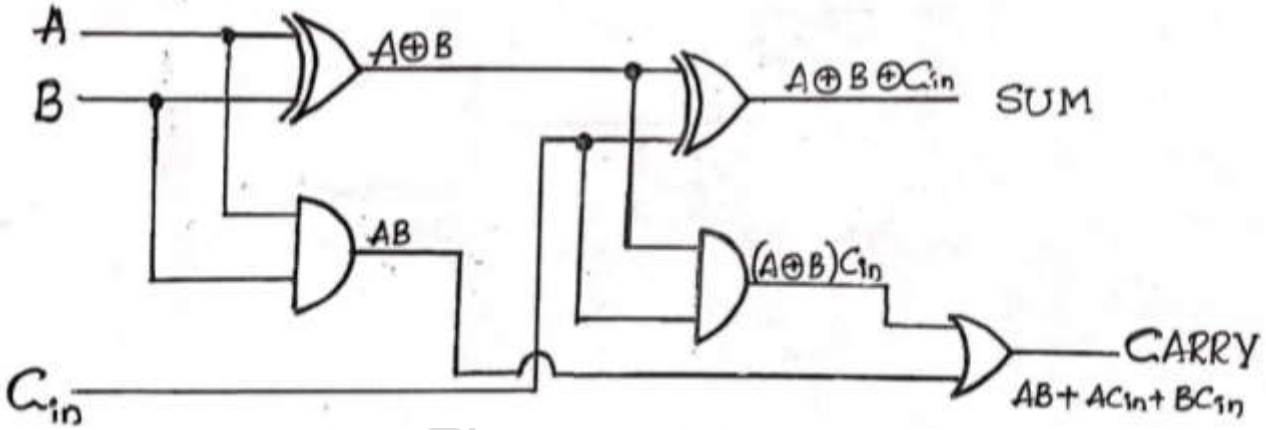
$Carry_{Out}$ $= \bar{A}BC_{in} + A\bar{B}C_{in} + AB\overline{C_{in}} + ABC_{in}$

$= AB + AC_{in} + BC_{in}$ *(Simplified final expression)*

Full adder Using Two Half Adder:

- Full adder can be realized using two half adders.
- The Half Adder1 Sum output is given as one of the input to the Half Adder2 with C_{in} as another input which gives the SUM of the full adder.
- The Half Adder1 carry is given as one of the input to the OR gate with carry of Half Adder2 which produces the $Carry_{Out}$ of full adder.





Sum $= \bar{A}\bar{B}C_{in} + \bar{A}B\overline{C_{in}} + A\bar{B}\overline{C_{in}} + ABC_{in}$

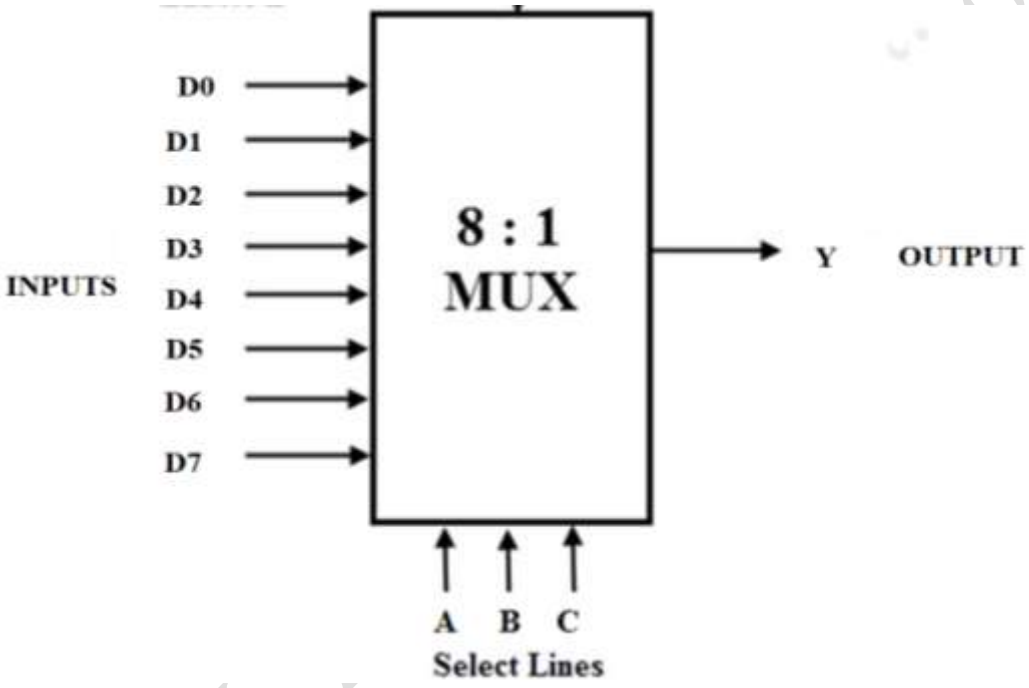
$= A \oplus B \oplus C_{in}$

$Carry_{Out}$ $= \bar{A}BC_{in} + A\bar{B}C_{in} + AB\overline{C_{in}} + ABC_{in}$

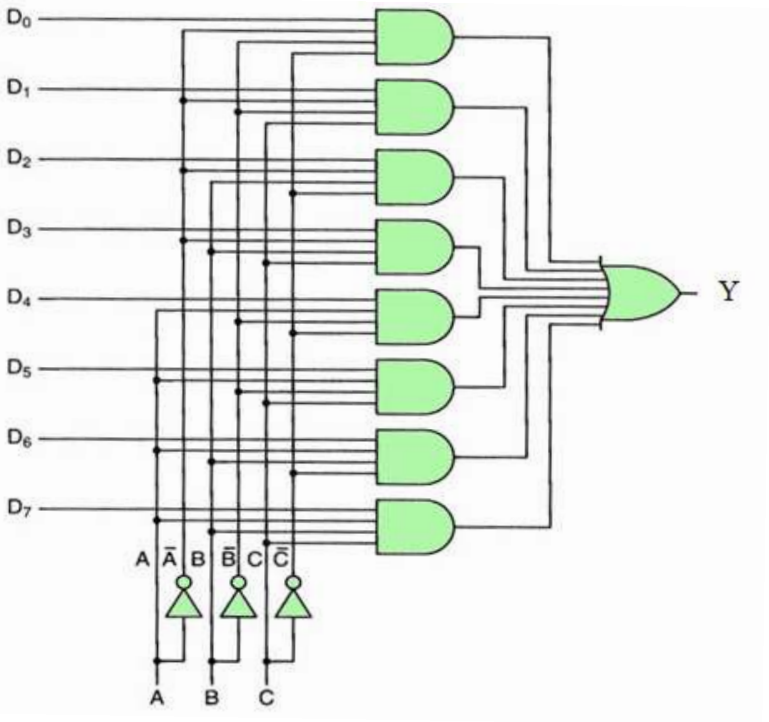
$= AB + AC_{in} + BC_{in}$

Multiplexers:

- The objective of a multiplexer is to select one signal from a group of 2^n inputs to be an output.
- 8:1 Multiplexer is as shown below; Lines D_0, D2, D3, D4, D5, D6, and D7 are the data input lines and Y is the output line.
- Lines A, B and C are called the select lines. They are three bit binary numbers which are used to choose one of the D input lines to be output on the line Y.
- 8:1 multiplexer diagrammed as shown in figure (a) and gate level diagram using AND and OR gates is as shown in figure (b).
- Suppose if D_5 is to be on output line, i.e. $Y=D_5$, then the corresponding select inputs are 5 = 101 or $A\overline{B}C$, similarly for $Y=D_3$, 3 = 011 or $\overline{A}BC$.
- The output Y will be the sum of all the $8(2^3)$ inputs.

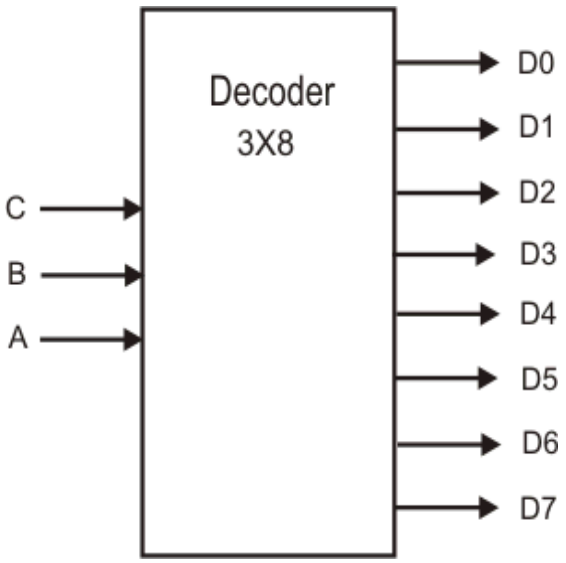


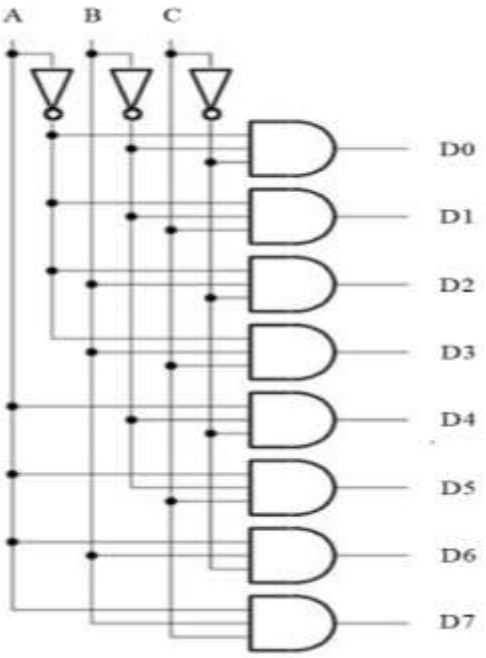
Select Data Inputs			Output
A	B	C	Y
0	0	0	D_0
0	0	1	D_1
0	1	0	D_2
0	1	1	D_3
1	0	0	D_4
1	0	1	D_5
1	1	0	D_6
1	1	1	D_7



Decoders:

- The objective of the decoder is to decode an n-bit binary number, producing a signal on one of the 2n output lines.
- Figure (a) shows the 3:8 decoder and the gate level diagram is as shown in figure (b) using AND gates.
- The same circuit is used as de-multiplexers.
- To produce D_6 as output, then inputs A=1, B=1, and C=0 or $AB\overline{C}$, similarly to produce D_2,inputs are A=0, B=1, and C=0 or $\overline{A}B\overline{C}$





Input			Selected Output							
A	**B**	**C**	**D_0**	**D_1**	**D_2**	**D_3**	**D_4**	**D_5**	**D_6**	**D_7**
0	0	0	**1**	0	0	0	0	0	0	0
0	0	1	0	**1**	0	0	0	0	0	0
0	1	0	0	0	**1**	0	0	0	0	0
0	1	1	0	0	0	**1**	0	0	0	0
1	0	0	0	0	0	0	**1**	0	0	0
1	0	1	0	0	0	0	0	**1**	0	0
1	1	0	0	0	0	0	0	0	**1**	0
1	1	1	0	0	0	0	0	0	0	**1**

If input is:

$\overline{A}BC$ = 011, the output is D_3

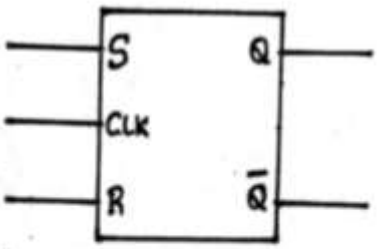
$AB\overline{C}$ = 110, the output is D_6

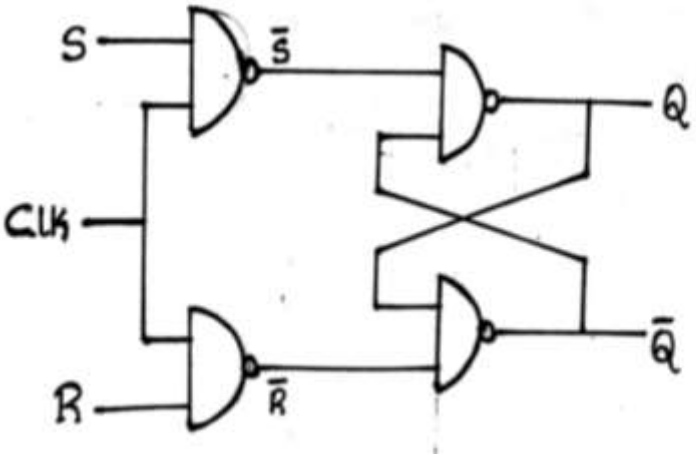
Flip-Flop:

- Flip flop is an electronic circuit that has two stable states and can be used to store One bit data. Flip flops are the basic memory elements of the sequential circuits.
- There are different types of Flip-Flops:
    1. SR Flip Flop
    2. D Flip Flop
    3. T Flip Flop
    4. JK Flip Flop

1. Clocked SR [Set-Reset] Flip Flop:

- The flip flop gets Set and Reset with the inputs.
- There are two states, Present (Q) and Next ($\overline{Q}$) state.
- When the clock pulse is LOW (0), for whatever the values of S and R, output remains unchanged.
- When clock pulse is HIGH (1), the flip-flop produces output for different values of S and R input i.e. as follows.
- When: Clk = 1, S=0 , R=0, Q=1, $\overline{Q}$=0
- When: Clk = 1, S=1 , R=0, Q=1, $\overline{Q}$=0, the flip flop gets **SET**
- When: Clk = 1, S=0, R=1, Q=0, $\overline{Q}$=1, the flip flop gets **RESET**
- When: Clk = 1, S=1, R=1, Q=0, $\overline{Q}$=0, the flip flop will be in the FORBIDDEN state.

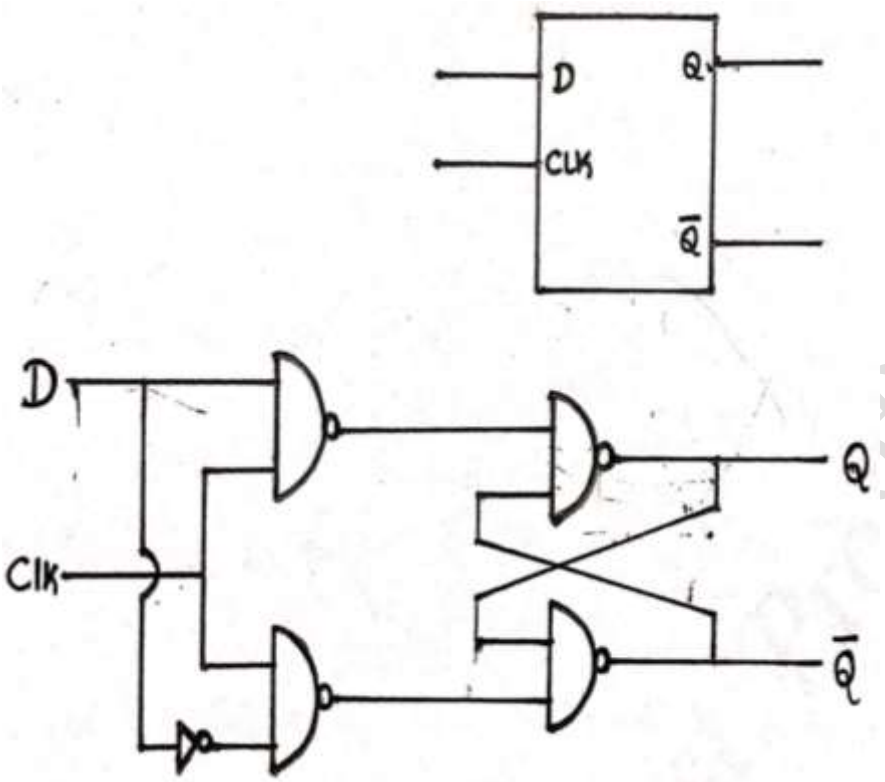




Clk	S	R	Q	$\overline{Q}$	STATE
0	X	X	Q	$\overline{Q}$	Previous State
1	0	0	Q	$\overline{Q}$	Previous State
1	0	1	0	1	Reset
1	1	0	1	0	Set
1	1	1	1	1*	Forebidden

2. Clocked D Flip Flop:

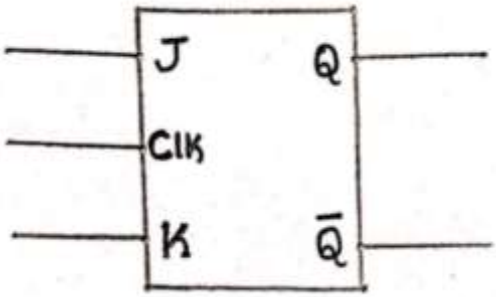
- D flip flop is the modification of the clocked SR flip flop.
- D input is given to S input and the complemented of the D input is connected to the R input of the clocked SR flip-flop.
- The D input is passed onto the flip flop when the value of Clk is 1 [Clocked Pulse is 1].
- When: Clk = 1, D = 0, Q = 1, $\overline{Q}$=0 the flip flop moves to SET state.
- When: Clk = 1, D = 1, Q = 0, $\overline{Q}$=1 the flip flop moves to RESET state.
- If the CP is 0, the flip flop switches to CLEAR state.

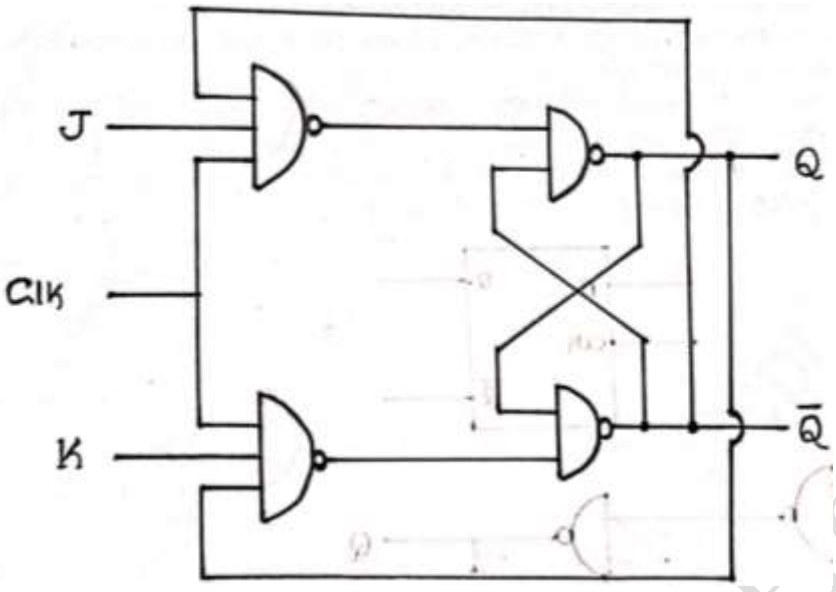


Clk	D	Q
0	X	Q (Previous State)
1	0	0
1	1	1

3. Clocked JK Flip Flop:

- It can also be defines as modification of the SR flip flop.
- The behaviour of inputs J and K is same as the S and R inputs of the SR flip flop.
- The letter J stands for SET and the letter K stands for RESET.
- When the clock pulse is LOW (0), for whatever the values of S and R, output remains unchanged.
- When clock pulse is HIGH (1), the flip-flop produces output for different values of S and R input i.e. as follows.
- When: Clk = 1, J = 0 , K = 0, Q=1, $\overline{Q}$=0
- When: Clk = 1, J = 1 , K = 0, Q=1, $\overline{Q}$=0, the flip flop gets **SET**
- When: Clk = 1, J = 0, K = 1, Q=0, $\overline{Q}$=1, the flip flop gets **RESET**
- When: Clk = 1, J = 1, K = 1, Q=0, $\overline{Q}$=0, the flip flop will be in the TOGGLE state.
- When both J=1, K=1, the flip flop switch the complement state. i.e. when Q=1, it switches to Q=0, and for the value of Q = 0, it switches to Q=1.

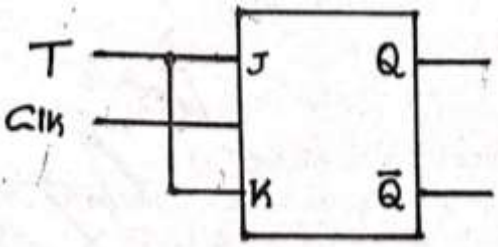


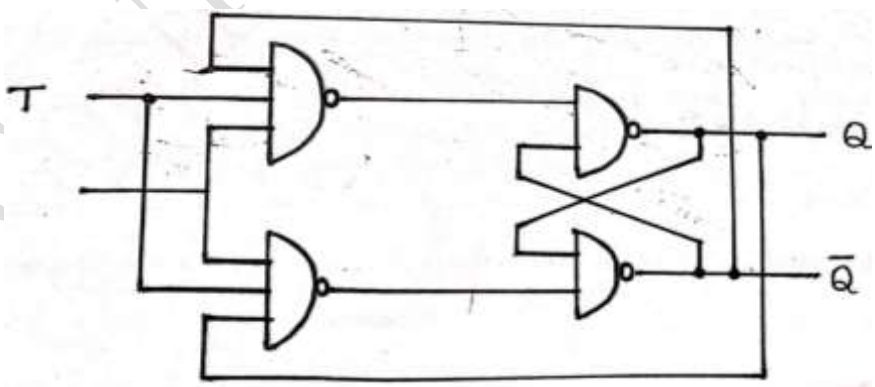


Clk	J	K	Q	STATE
0	X	X	Q	Previous State
1	0	0	Q	No Change
1	0	1	0	Reset
1	1	0	1	Set
1	1	1	$\bar{Q}$	Toggle

4. T Flip Flop:

- It is the simple form of the JK flip flop.
- Both the J and K inputs are connected together and thus are also called a single input JK flip flop.
- When the clock pulse is given to the flip flop, the output begins to Toggle.

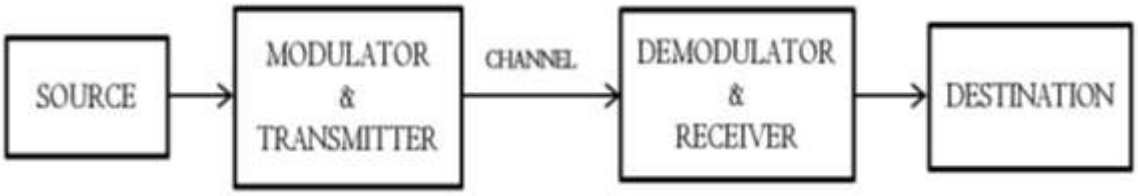




Clk	T	Q
0	X	Q (Previous State)
1	0	Q (Previous State)
1	1	$\bar{Q}$

Elements of Communication Systems:

Communication is the process of transferring of information from one point to another point through the channel or a medium.



Information Source:

- It generates the message or the information to be transmitted. These messages are non-electrical signals.
- Eg: Text, Voice, Videos etc.

Modulator and Transmitter:

- Modulator is an electronic device, which converts the non-electrical signal into electrical signal suitable for transmission over a channel.
- It consists of Transducer, Encoder, Amplifier, and Modulator to make the signal suitable for transmission.

Channel:

- Channel is a medium through which the electrical signal is transmitted from one place to another.
- Communication channel can be wired (Co-axial cable, OFC, Twisted pair cable) or wireless.

Noise Source:

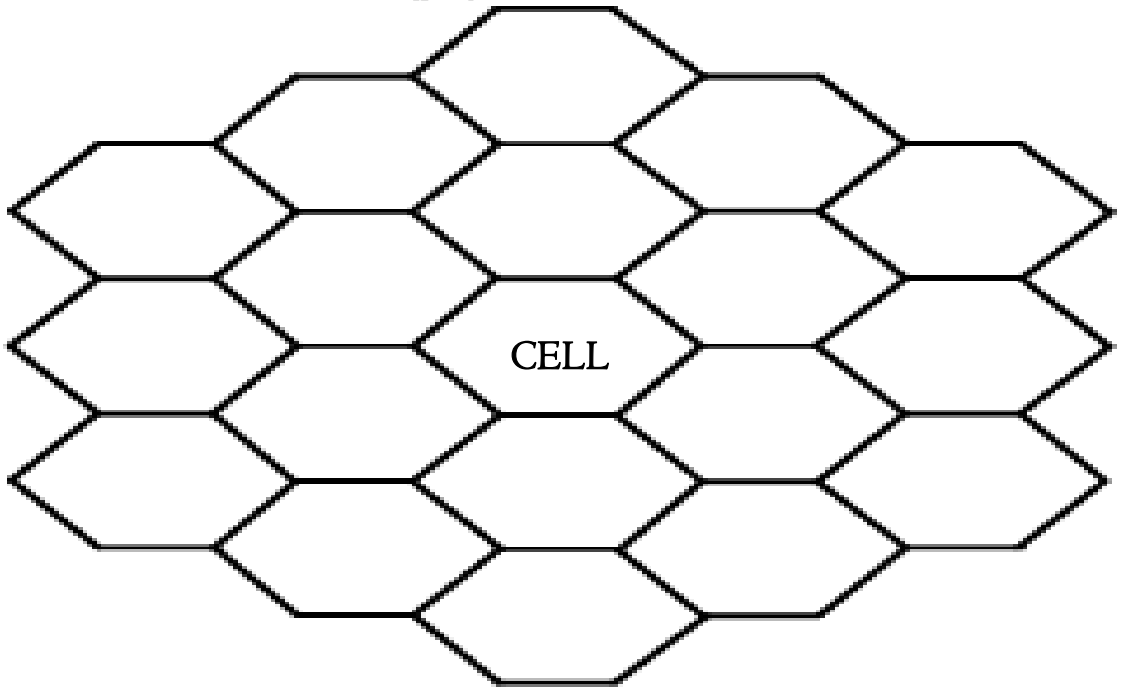
Noise is an unwanted signal that gets added to the message signal during transmission over the channel. Noise may be natural or man-made.

Receiver and Demodulator:

- It is a collection of electronic circuit designed to convert the modulated signals back to the original information.
- It consists of transducer, decoder, amplifier, demodulator to get original signal from electrical signal and received at the destination.

Principle of operations of Mobile Phone:

- A cellular/mobile system provides standard telephone operation by full-duplex two-way radio at remote locations.
- It provides a wireless connection to the **Public Switched Telephone Network (PSTN)** from any user location within the radio range of the system.
- The basic concept behind the cellular radio system is that rather than serving a given geographical area within a single transmitter and receiver, the system divides the service area into many small areas known as **Cells**.
- The typical cell covers only several square kilometres and contains its own receiver and low-power transmitter.
- The cells area is an ideal Hexagon. But in reality they will have circular or other geometrical shapes.
- These areas may overlap and cells may be of different sizes.
- A basic cellular system consists of mobile stations, base stations and a Mobile Switching Center (MSC), which is also known as Mobile Telephone Switching Office (MTSO).
- These MTSO controls the cells and provides the interface between each cell and the main telephone office.
- Each mobile station consists of a *transceiver*, an antenna and control circuit.
- The base station consists of several transmitters and receivers which simultaneously handle full-duplex communication.
- The base station serves as a bridge between all mobile users in the cell and connects the simultaneous mobile call via telephone lines or microwave link to the MSC.
- The MSC co-ordinates the activities of all the base stations and connects the entire cellular system to the PSTN.
- Most cellular system provides a service known as *roaming.*



Cellular telephone Unit:

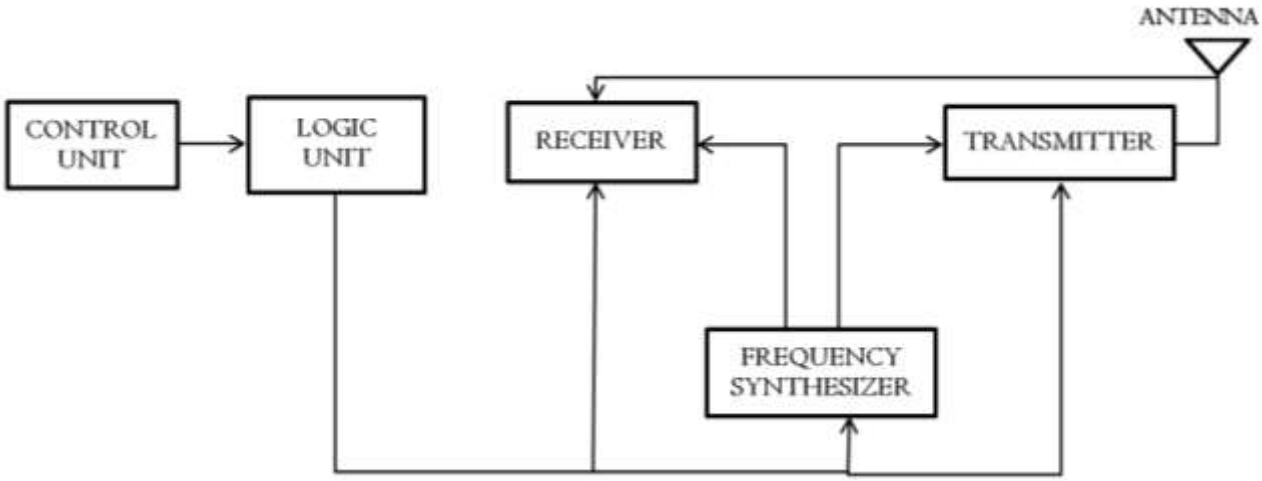


Figure above shows the block diagram of a cellular mobile radio unit. The unit consists of 5 major blocks.

1. Control unit.
2. Logic unit
3. Receiver
4. Frequency Synthesizer
5. Transmitter

Control Unit:

The control unit is a set of speakers, microphone with touch tone dialling facility and it stores the memory like numbers and dialling features.

Logic Unit:

Logic unit is micro-processor controlled master control circuit for cellular radio. It basically controls the complete operation of MTSO and mobile unit.

Receiver:

Receiver consists of RF amplifier, FM demodulator and filters. An RF amplifier boosts the level of received cell site signal. Received signal is monitoring by MTSO. If the signal is weak in the present cell, then the mobile unit is shifted to other site where the signal is strong.

Frequency Synthesizer:

It is used to generate various signals required for transmitter and receiver. When a mobile unit initiates a call, MTSO identifies the user and assigns a frequency Channel which is not used by any other mobile in the cell. MTSO sends a unique code for setting channel frequencies.

Transmitter:

It is a low power FM transmitter operating in a frequency range of 825 to 845 MHz. There is a 66.63MHZ transmit channel. The modulated output is translated up to final transmitter frequency with the help of a mixer, whose second input comes from the frequency synthesizer. The basic feature of high power translator is that output is controllable by the cell site and MTSO.